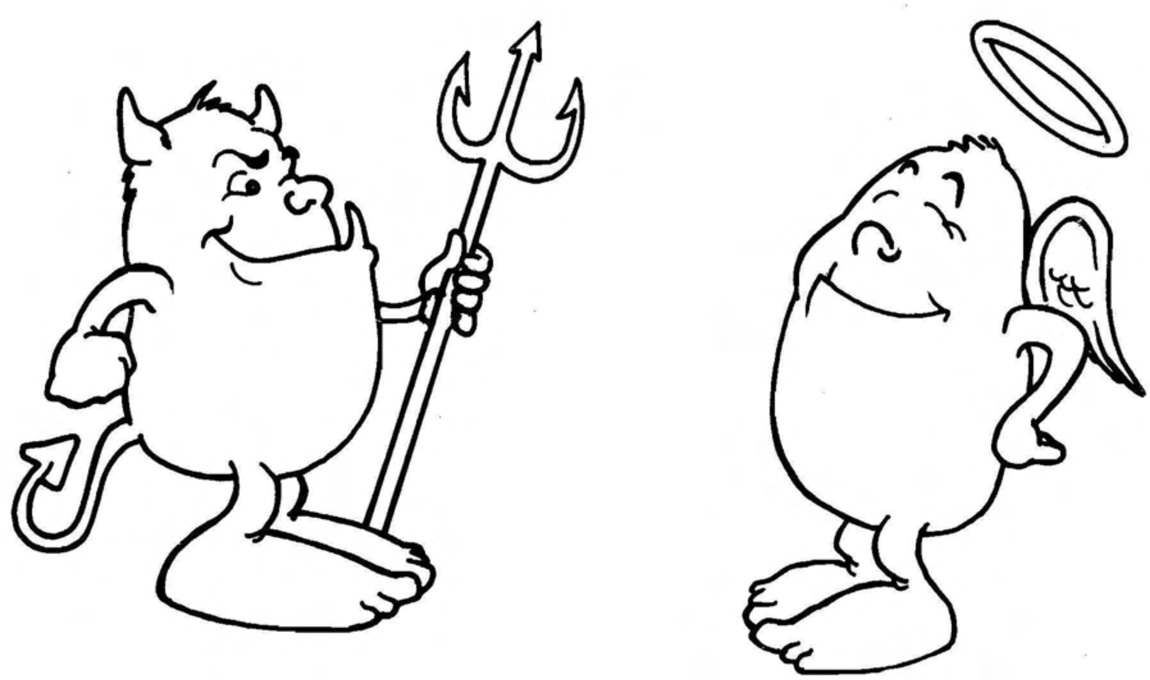
# Pepper II™

## Operation and Service Manual 2ND Edition



# PEPPER II™

Operation and Service Manual
2nd Edition


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This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instruction manuals, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

# EXIDY PEPPER II™
# OPERATION AND SERVICE MANUAL

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# FOREWORD

Part One of this manual is on Preliminary Procedures, describing game inspection, installation, and checkout. Also, adjustment procedures are given for power supply, audio volume, and Selectable Options.

Part Two, Modes of Operation, describes the four PEPPER II modes: Automatic Self-Diagnostic Test Mode, Attract Mode, Game Play Mode, and Vanity Mode.

Appendix A contains game schematics, with a circuit description on the page opposite them.

Appendix B is the Illustrated Parts List. Parts are pointed out in the drawings and listed opposite each drawing.

# I. PRELIMINARY PROCEDURES

## A. GAME INSPECTION

All Exidy equipment is carefully packaged in well-padded cardboard containers to prevent damage during shipment. **Before** signing the delivery receipt, you should follow this procedure:

1. Check for obvious damage and make certain that the physical piece count of the shipment matches the piece count on the bill of lading. These two procedures should always be done **before** signing the delivery receipt.

2. Shortages and/or obvious damage to the packaging on any given shipment should be noted **in writing** on the delivery receipt **before** signing for the delivery.

3. If concealed damage is suspected on any shipment, those packages believed to contain the damaged goods **should be opened in the presence of the delivery driver.** If the goods have sustained concealed damage, a description of said damage should be noted **in writing** on the delivery receipt **before** signing for the delivery.

4. **Never** apply power to any game with noticeable damage.

### 1. Filing a Claim

To file a claim, follow this procedure:

1. Any and all damaged freight, including packaging, **should be retained by the consignee** until a physical inspection of said freight can be made by a representative of the carrier involved.

2. The Claims Manager for the carrier involved should be notified as soon as possible, after the damaged goods are received. Preferably, the carrier's Claims Manager should be notified within forty-eight (48) hours of receipt of the goods by the consignee.

3. If warranted, a written claim should be filed with the carrier involved. A detailed description of the damage(s) should be provided and copies of all supporting documents, **including bill of lading and/or delivery receipt, inspection report, and invoice**, should be attached.

4. The sooner a claim is filed, the better for all parties concerned. The carrier against which a claim is filed is required, by law, to respond to (acknowledge) that claim within thirty (30) days of receiving same and must reach a final disposition in the matter within one hundred twenty (120) days.

### 2. Visual Inspection

1. Remove the rear access door with the appropriate packaged key.

2. Examine each major and electrical component thoroughly for scrapes, dents, broken or missing parts and loose or missing screws.

3. Check for loose cable connectors.

4. Visually verify that all the integrated circuit devices (IC's) plugged into sockets are properly seated and that no IC pins are bent or misaligned.

If you find any damage during this inspection, file a claim with the carrier. Send a complete report of the damage to Exidy Inc.

## B. INSTALLATION

Planning the location of the game should involve both physical and electrical considerations. Such physical considerations concern the placement of the equipment with respect to these clearances:

Height: 72.50 inches, 184.2 cm.
Width: 25.50 inches, 64.8 cm.
Depth: 31.00 inches, 78.7 cm.

An indoor, relatively dust-free environment is necessary, with proper conditions required of any electrical component. Electrical considerations include availability of an AC outlet with the correct voltage and frequency. You should consider the working space required for technicians and operators incuding access to the rear of the game.

NOTE:

The cabinet must be within five feet of an AC outlet. Be certain that a ground jack or terminal is available at the outlet.

CAUTION:

DO NOT remove the AC ground prong from the plug. Doing so **voids your warranty!**

## C. PRELIMINARY CHECKOUT PROCEDURE

After properly installing PEPPER II™, we suggest following this procedure to check its operation:

1. Plug the AC jack into the AC outlet.

2. Once powered up, after five seconds of silence, a quick beep sounding like an organ chord, is heard. This is part of the Exidy Audio Diagnostic Test. A single beep indicates all is well with the audio board. If more than one beep is heard, consult Part II, Automatic Diagnostic Test Mode.

3. Allow 8-10 seconds to pass for the CRT to warm up.

4. Observe the TV monitor display to assure the correct attract mode is present on the screen, as described in Part II B, Attract Mode. If the PEPPER II™ display is incorrect, contact Exidy Customer Service Department.

5. Insert the appropriate coin or token into either of the coin slots. All the messages in the attract mode will flash the following line:

PRESS PLAYER ONE START
or
PRESS ONE OR TWO PLAYER START

depending on the number of coins dropped into the coin slot.

6. Press one or two player start and play the game to verify that all screen images are displayed as described in Part II D, Game Play Mode.

NOTE:

Screen colors may possibly be affected by the relative position of the game with respect to the earth's magnetic field. If this condition occurs on your game we suggest rotating the game to the RIGHT or LEFT. Also, by powering the game ON and OFF, the internal degaussing unit should eliminate any color deficiencies. In the event that this does not correct the monitor colors, externally degaussing the game will eliminate the affected colors.

If assistance or repairs are necessary, contact the Exidy Customer Service Department, (800) 538-8402.

## D. ADJUSTMENTS

### 1. Power Supply Information and Adjustments

All DC Power required to operate PEPPER II™ is supplied in the Exidy Power Supply Module. These supply outputs are as follows:

| | | |
|---|---|---|
| +5v DC | @ | 6 amps |
| -5v DC | @ | 1 amp |
| +12v DC (HI)* | @ | 3 amps |
| +12v DC (HI)* | @ | 1 amp |
| -12v DC (HI)* | @ | 3 amps |
| -12v DC (LO)* | @ | 1 amp |

* (HI) refers to 'high current'
* (LO) refers to 'low current'

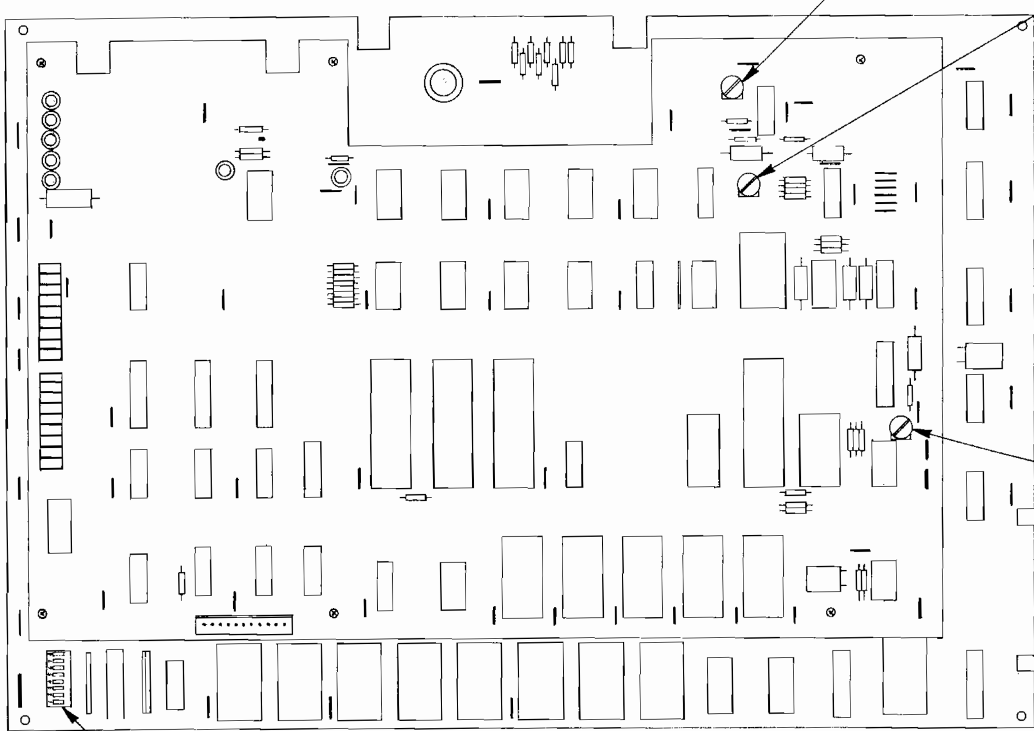
CAUTION: Only certified technicians should make adjustments on all components of PEPPER II™. AC line voltage selection is available in your PEPPER II™ game by setting the appropriate jumpers on the power chassis. Only the +5v DC is adjustable. This must be adjusted to:

+5.00v DC +/- .25v

as measured on the PCB near the microprocessor (location 2A).

### 2. Audio Board Adjustments

The following drawing points out the three individual audio adjustments and the location of the DIP switch. The audio board rides piggyback on the logic board, mounted on the right wall of the game, when viewed from the rear service door.




### 3. Operator Selectable Options

PEPPER II™ has several switch selectable options controlled by an 8-position DIP switch located on the main logic board at position 16A. This switch is accessible through the back door of the game.

PEPPER II™ is shipped with the dip switch already set for optimum dollar return. Should you decide to change the settings, you may select any of the following options by setting the proper switch accordingly:

| a. COINAGE | Switch 4 | Switch 5 | Switch 8 |
|---|---|---|---|
| 1 Coin - 1 Credit | OFF | OFF | OFF |
| 2 Coins - 1 Credit | OFF | ON | OFF |
| 1 Coin - 2 Credits | ON | OFF | OFF |
| 1 Coin - 4 Credits | ON | ON | OFF |
| 1 Coin - 3 Credits OR 2 Coins - 7 Credits | OFF | ON | ON |

a. COINAGE (continued)

| | Switch 4 | Switch 5 | Switch 8 |
|---|---|---|---|
| 1 Coin in Left Slot-1 Credit, 1 Coin in Right Slot- 5 Credits | OFF | OFF | ON |
| 1 Coin in Left Slot-1 Credit, 1 Coin in Right Slot- 4 Credits | ON | OFF | ON |
| 2 Coins in Left Slot-1 Credit,1 Coin in Right Slot- 3 Credits | ON | ON | ON |

b. NUMBER OF TURNS

| | Switch 6 | Switch 7 |
|---|---|---|
| 2 Turns | OFF | OFF |
| 3 Turns | ON | OFF |
| 4 Turns | OFF | ON |
| 5 Turns | ON | ON |

c. BONUS TURNS (Extra turn awarded when selectable number of points are made. Maximum of 2).

| | Switch 2 | Switch 3 |
|---|---|---|
| 40,000 | OFF | OFF |
| 50,000 | ON | OFF |
| 70,000 | OFF | ON |
| 90,000 | ON | ON |

**NEW!! 2 Distinct Options**

The following two features have been added to facilitate the many different needs of Exidy game operators. If either of these are chosen, the game is set for three turns, 1 coin 1 credit, and 70,000 bonus.

**FREEPLAY:** For those wishing to demonstrate PEPPER II, a freeplay mode may be achieved by turning switches 2 through 8 ON.

**STRIPPED MUSIC:** For those locations desiring limited audio effects, this option plays limited selections of game music and effects. Turn switch 2 OFF, and switches 3 through 8 ON.

**WARNING:** Anytime switches 2-8 are ON, the game will play in freeplay. Anytime switches 3 through 8 are ON with switch 2 OFF, the game will play with stripped music.

## II. MODES OF OPERATION

### A. AUTOMATIC SELF-TEST MODE

PEPPER II™ automatically tests the logic and audio boards on power up. To run the Control and Color Test, activate the coin switch while powering up.

You may bypass both diagnostic modes by depressing either the one or two player start button while powering up. After 8 seconds of the message 'STAND BY VERSION X', (where X is a number representing the software version) the Attract Mode appears.

### 1. LOGIC DIAGNOSTIC TESTS

#### a. The RAM Test

When PEPPER II™ is first turned on, a processor and video RAM test is done. If the RAM passes, it goes immediately into the ROM test, without a message indicating it passed the RAM test.

If a RAM chip fails, an attempt is made to indicate the RAM chip where a failure was detected. Since the screen depends on a properly functioning RAM, this indication may not be displayed. A failed RAM may be indicated by a digit from 0 to 7 in every position on the screen using four colors. The code for these digits is as follows:

| Number on Screen | RAM chip to check | | Number on Screen | Location on Plane Interface Board | |
|---|---|---|---|---|---|
| 0 | 5A | Processor RAM | 8 | U1 | Off Logic |
| 1 | 4A | failure | 9 | U1 | failure |
| 2 | 8B | Screen RAM | A | U1 | RAM |
| 3 | 7B | failure | B | U1 | failure |
| 4 | 9C | | | | |
| 5 | 9C | Video RAM | | | |
| 6 | 9C | failure | | | |
| 7 | 9C | | | | |

The RAM test cycles if the failure is persistent.

#### b. The ROM Test

If the RAM test passes, the ROM test begins. The message STAND BY VERSION N appears on the screen (where N is a number). One by one, 'X''s appear on the screen. Each X indicates half (2K) of a ROM board chip, numbered 6A through 13A, has passed the diagnostic test. After all marks appear, the game then goes into the Attract Mode, indicating all is well.

If any failure is detected during the ROM test, a hex digit appears instead of an exclamation point with a 'BAD ROM' message at the top of the screen. The test repeats indefinately if a bad ROM is encountered. The key for which chip to check is as follows:

Message: ROM Chip to check:

| MESSAGE: | | | CHIP TO CHECK: |
|---|---|---|---|
| 8 prom | 7 prom | 6 prom | |
| 0 | | | lower 2K of 13A |
| 1 | | | upper 2K of 13A |
| 2 | 0 | | lower 2K of 12A |
| 3 | 1 | | upper 2K of 12A |
| 4 | 2 | 0 | lower 2K of 11A |
| 5 | 3 | 1 | upper 2K of 11A |
| 6 | 4 | 2 | lower 2K of 10A |
| 7 | 5 | 3 | upper 2K of 10A |
| 8 | 6 | 4 | lower 2K of 9A |
| 9 | 7 | 5 | upper 2K of 9A |
| A | 8 | 6 | lower 2K of 8A |
| B | 9 | 7 | upper 2K of 8A |
| C | A | 8 | lower 2K of 7A |
| D | B | 9 | upper 2K of 7A |
| E | C | A | lower 2K of 6A |
| F | D | B | upper 2K of 6A |

## 2. AUDIO DIAGNOSTIC TESTS

While the Logic tests are underway, the Audio board is also being checked.

Five seconds after power on, one or more quick beeps, like an organ chord, are heard. This is part of the Exidy Audio Diagnostic Test. The number of beeps that sound indicate different conditions of the Audio board. The following code is an indication **only**, of where to first check the Audio Board. Because this diagnostic test only evaluates certain components, other circuitry is relied upon for the test. Should this other circuitry fail, the diagnostic test may not, then, point directly to the failure. Please use the results of this test as a guideline for further troubleshooting.

The code is as follows:

0 beep: If no beeps are heard, along with a hum or random notes, this may indicate a failure in 3A and/or 7A.

1 beep: All audio hardware is OK. However, be sure to check the Attract Mode Cycle anyway for a possible message to check the Audio Board. In occasional instances, this can occur. The message will further direct you.

2 beeps: ZERO PAGE RAM failure. Check 6532 RAM I.O. Timer Array at location 7B on the board.

3 beeps: (will not occur)

4 beeps: ROM failure

5 beeps: INTERRUPT failure. Check 6532 at location 7B.

In addition, this message appears during the Attract Mode **only** if the Audio Board needs to be checked:

'CHECK AUDIO BOARD'

XX YY

XX and YY in the message are code characters defined as follows:

XX= 01 = ZERO PAGE RAM FAILURE, check 6532

02 = (will not occur)

n3 = ROM FAILURE. Any number in the XX position ending with a 3 (for example, 23, 33, etc.) indicates a ROM failure. The first digit (2 and 3 in the previous example) points you to the appropriate chip that needs to be checked. The code for the any number ending with 3 in the XX position is as follows:

| XX= | Chip to Check |
|---|---|
| 03 | 3A |
| 13 | 4A |
| 23 | 5A |
| 33 | 6A |
| 43 | 7A |

Note: The message reflects the first bad chip it encounters, in numeric order. It is possible for chips following it to also be bad.

04 = INTERRUPT FAILURE, check 6532.

?? = FAULTY COMMUNICATIONS. Check 6520 at 9B.

Here is the code for the second two numbers in the YY position.

YY= 40 = Communication **from** Logic Board **to** Audio failed. Check 6520, both locations 8B and 9B.

80 = Communication **to** Logic Board **from** Audio failed. Check 6520, at locations 9B and especially 8B.

<0 = Communication between Logic and Audio failed. Check 6520, both locations 8B and 9B.

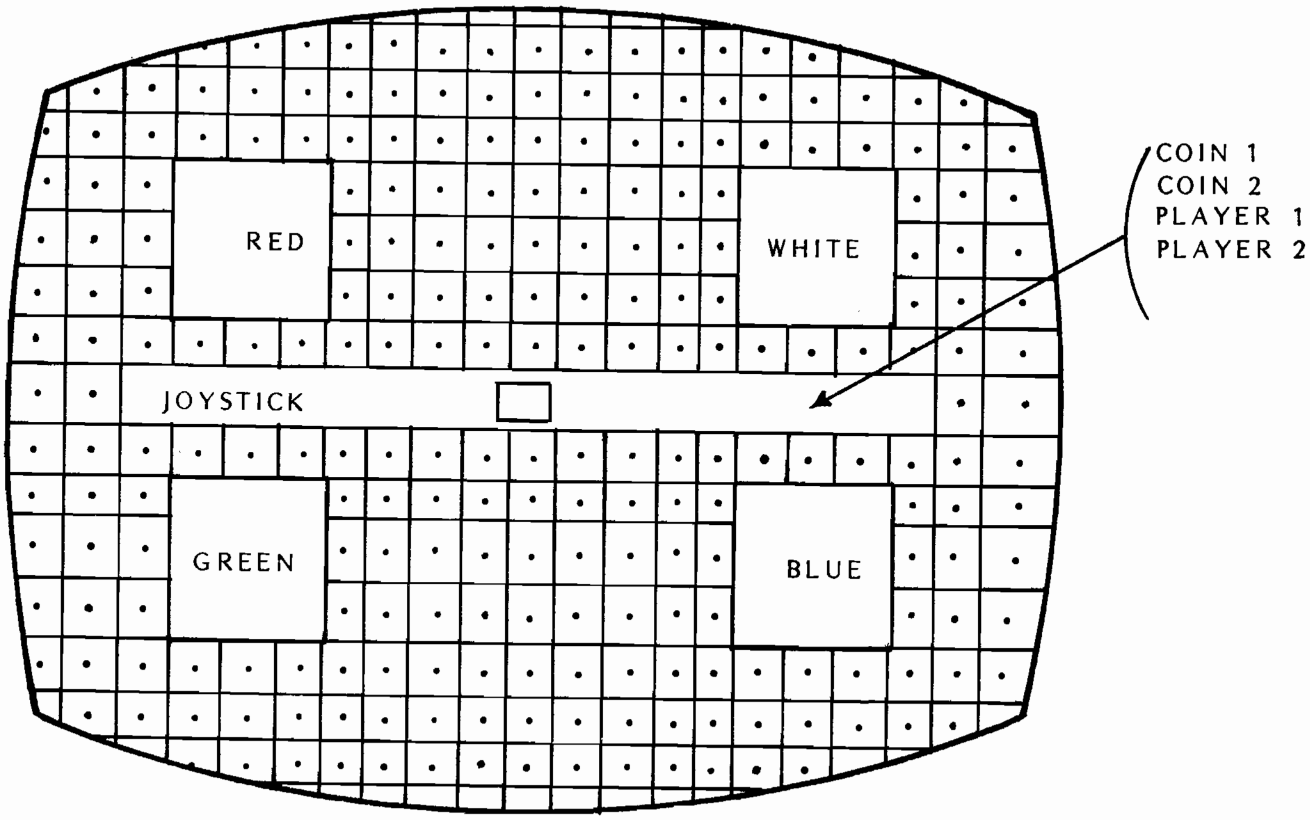
Also, the symbol <0 in both the XX and YY position, along with a hum or random notes and no beep after power on, may indicate a failure in 3A and/or 7A.

## 3. CONTROL AND COLOR DIAGNOSTIC TESTS

If desired, you may test all player controls and screen colors. To do so, activate either

coin switch at power-up. The game then enters the Control/Color Test Mode. This mode lasts for seven minutes to give you time to test and make adjustments. After that, the Attract Mode begins.

In the Control/Color Test Mode, the screen shows this pattern:




The grid pattern tests your screen for any distortion or convergence.

The solid blocks of color (red, white, green, and blue) allow you to adjust the color. When any player control (player 1 start, player 2 start, or Fire) or coin switch (coin 1 or coin 2) is activated, its name appears below the white box. This shows that the switch connection is proper. When the joystick is activated, the message Joystick appears below the red box. Also, in the middle of the screen, a square indicates the joystick direction.

## B. THE ATTRACT MODE

After PEPPER II goes through its automatic self-diagnostic test mode on power-up, a series of screen displays are shown repeatedly. One screen gives instructions to the player, another shows a brief demonstration of game play, and a third shows the High Score Table, reset to factory scores each time PEPPER II is powered up.

## C. INTRODUCTION MODE

After depositing a coin, this message blinks on the screen while the Attract Mode

continues:

PRESS PLAYER ONE START

If enough coins for two plays are deposited, this message appears:

PRESS ONE OR TWO PLAYER START

After one of the two play buttons are pressed, this message appears on the screen:

GET READY PLAYER 1

D. GAME PLAY MODE

Each play screen of PEPPER II shows a maze with exits leading to 3 other mazes. All four mazes must be filled to advance to the next level. To fill in a maze, the player guides 'Pepper' around a floorplan. As Pepper travels, he leaves a track or zipper. Once he encloses an area, it fills in and points are awarded.

The floorplan is flashed during the first four mazes to help the beginning player learn the game field quickly. After the first four mazes (level 1), the player must find his way around with only square markers giving clues.

**1. Obstacles and Hazards**

Pepper, the angel, must avoid two enemies: Roaming Eyes, and the pink 'WHIPPERSNAPPER' who unzips all 'freestanding' lines (those not enclosing an area). Pepper's one defense is to enclose an area containing a pitchfork, which turns him into a devil for a few seconds. At that time he can go after all Roaming Eyes for points. At the same time, the Whippersnapper freezes.

If Pepper backtracks on a freestanding line, it unzips. The player soon learns to maneuver Pepper around on the lines enclosing areas, to avoid losing freestanding lines to the WHIPPERSNAPPER.

The player goes to different mazes by going out any of four exits, located in the middle of each side of the screen. As each maze is filled in, the box which represents it on the screen (marked 1, 2, 3, and 4) fills in. When all four mazes are filled in, a 'Super Bonus' is awarded, a new level is given, and a cube appears on the bottom of the screen.

**2. Scoring**

Points are made for enclosing a space (the larger the room, the more points earned), hitting a pair of roaming eyes when energized, obtaining prizes, completing a maze, and completing 4 mazes (one level). A bonus turn is awarded at the operator selectable score of 40,000, 50,000, 70,000 or 90,000.

**a. Prizes**

A prize appears on each maze for a brief period. The player must enclose the area it appears in to gain the prize and points, and then the prize is shown beneath the maze. If the player does not get the prize while it appears, it appears again on a different maze. Only the most recent prize obtained appears at the bottom of the screen.

### b. Energizers

Energizers are seen in different areas as a pitchfork and halo symbol. When PEPPER encloses a room containing this symbol, he turns into a devil for four seconds and may then go after all roaming eyes for points. A deluxe energizer occaisionally appears in the area at the center of the maze. Here, the pitchfork/halo symbol alternates with the deluxe energizer symbol every few seconds. If PEPPER encloses the middle area when the deluxe energizer appears, the Whippersnapper disappears for a few seconds, while PEPPER may pursue Roaming Eyes for points.

After four mazes (level 1) is complete, subsequent deluxe bonuses make the Whippersnapper disappear for a few seconds, while the Roaming eyes disappear for 2 seconds. The PEPPER is a devil for four seconds.

## E. VANITY MODE

Anytime a player's score exceeds one of the five current high scores, he is eligible to enter his initials in the Vanity Table. If both players of a two player game are record high scorers, the highest of the two is first invited to enter his initials. To do so, he directs a character through the alphabet with the joystick. Once on the letter desired, he hits either of the Start buttons. After either logging his initials, or after about 45 seconds, the game returns to the Attract Mode.

## APPENDIX A: SCHEMATICS

### MEMORY MAP

| Hex Address | Function or Device |
|---|---|
| FFFA-FFFF | Interrupt and Reset Vectors |
| 8000-FFF9 | Program memory space |
| 52XX | Audio board communications |
| 5103 | Interrupt Condition Latch (read) |
| 5101 | Control Inputs Port (read) |
| 5101 | Output Control Latch (write) (Not used in PEPPER II™ upright) |
| 5100 | Moving Objects Image Latch (write) |
| 5100 | Option Dipswitch Port (read) |
| 50C0 | Moving Object 2 Vertical Position Latch (write) |
| 5080 | Moving Object 2 Horizontal Position Latch (write) |
| 5040 | Moving Object 1 Vertical Position Latch (write) |
| 5000 | Moving Object 1 Horizontal Position Latch (write) |
| 4800-4FFF | Character Generator RAM |
| 4000-43FF | Screen RAM |
| 0200-03FF | Scratchpad RAM |
| 0100-01FF | Stack RAM |
| 0000-00FF | Zero Page RAM |
| 6000-67FF | Character Generator RAM |
| 6800-6FFF | Character Generator RAM for multicolors |

## PAGE 1, GAME LOGIC PCB

1. Master Oscillator (1D)

From this oscillator all dynamic operations are derived, such as the processor clock, the main element and line counters, the shift register clocks, as well as all other forms of timing signals.

2. Element (Horizontal) Counters (1C, 1E, 2E)

These components form the final stages of horizontal timing. All operations in this game requiring horizontal positioning or timing have their origin here. Note that, beginning with signal HCLK (from Clock Divide Counter 2D), there are 256 counts prior to setting signal E256 high. When this signal goes high, it indicates that the horizontal blanking period is in progress. At this time the final counter (1E) is preloaded with a higher number than previously loaded. This creates a shorter count the second time around. The shorter count measures the retrace interval. When the retrace count is finished, the counter preloads with a lower number, establishing a longer count sequence again for 'real time' sweep of the electron beam across the face of the CRT.

3. Line (Vertical) Counters (4F, 5F, 6E)

These components form the entire vertical timing operation starting with a clock derived from horizontal timing. These counters count 256 times and then preload with a higher number, causing a shorter count the second time. This shorter count measures the vertical retrace interval. Note that signal L256, when high, indicates vertical blanking is in progress. After the completion of the vertical retrace count, the counters once again preload with a lower number. This way they count 256 times during the sweep of the electron beam down the face of the CRT, allowing the horizontal timers to sweep one complete horizontal line for each count of the vertical counters. Thus, the electron beam reaches the bottom of the CRT, after completing 256 horizontal line sweeps. It then begins the vertical retrace count, and the whole cycle begins anew with the beam starting again at the top of the CRT.

4. Screen RAM Addresses (7D)

During the time the screen RAM is examined by the logic for output to the monitor screen, addresses must be applied to the screen RAM to count up at a rate corresponding to the image cells conceptually arranged on the screen in a 32 x 32 matrix. The counts used here, 4 from the element counters, and 4 from the line counters, fulfill this timing requirement. The least significant element count used (E8) represents an interval exactly eight times that of one element. The least significant line count used represents an interval exactly eight times that of one horizontal line, or eight times a single line count. Dividing a 256 element line by 8 yields 32, and likewise dividing a 256 line vertical sweep by 8 yields 32. Thus the screen RAM address lines (RAMØ through RAM9) count at a rate that creates 32 horizontal counts and 32 vertical counts as the electron beam sweeps the face of the CRT. This makes 1024 conceptual 'image cells' into which can then be inserted images of 8 elements by 8 lines. For more information concerning these images, refer to the text for pages 2 and 3 of the Logic Schematics.

5. Coin Input Decoding (1H)

Some models of PEPPER II™ contain two separate coin inputs for special coinage applications. NOR gate 1H combines these separate inputs, making signal 5COINT, which sets the interrupt flip-flop (6E on page 8) when either coin input becomes active, thus forcing the microprocessor to jump to the interrupt service routine. This interrupt driven operation prevents ever missing a coin when inserted. However, this also means that when a game is first powered up, the coin input must be inactive. If for some reason the coin input switch is enabled at the time of power up, the game does not properly initialize until the switch is disabled.

6. Hardware Generated Line Positioning Proms (3E, 4E)

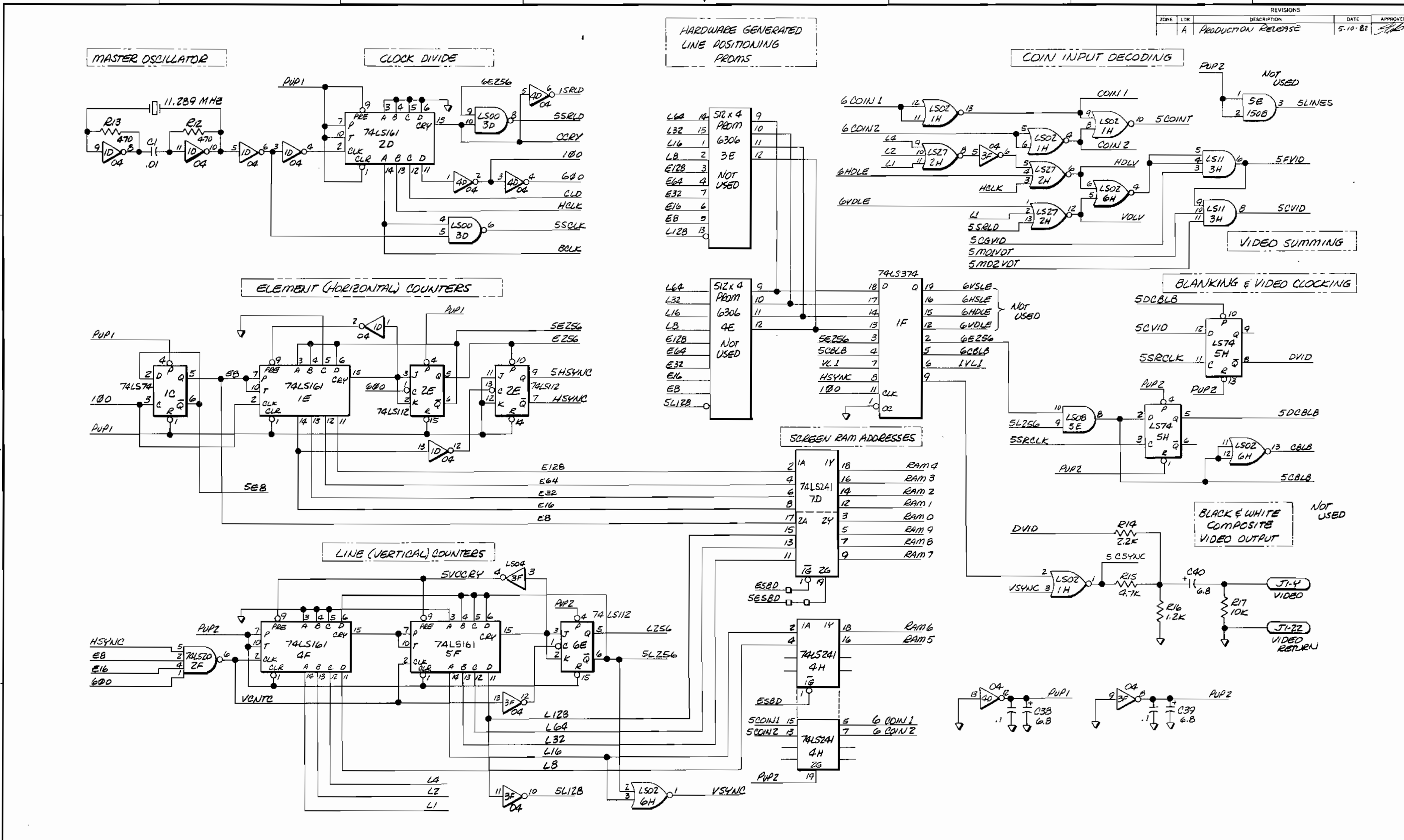
These PROMs are not used for PEPPER II™.

7. Blanking and Video Clocking (5H)

Flip-flop 5H merely combines blanking and all other video.

8. Black and White Composite Video Output (1H)

This circuit is not used for PEPPER II™. If desired, however, these components may be installed to aid troubleshooting, by acting as a 'video probe'.




| | | | |
|---|---|---|---|
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| 390 JAVA DR SUNNYVALE CA 94086 408-734-9410 | SIZE D | TITLE/DESCRIPTION 6502 GAME LOGIC PCB PEPPER II SYNC AND VIDEO GENERATION | DRAWING NO. 77-0008-01 REV A |

1. Screen Controller PROM (6D)

This PROM controls the direction of data flow into and out of the screen RAM and character generator RAM. It prevents timing errors and buss conflicts, assuring that the microprocessor can write to either the screen or character generator RAM, or read back from either.

2. Screen RAM (7B, 8B)

The screen RAM is comprised of two 1024 x 4 static RAMs, configured to act as a single 1024 x 8 RAM. This creates a screen matrix of 32 horizontal by 32 vertical positions. A single byte code is stored in each of these positions to represent a particular character. During 'real time' (the time the CRT is being swept by the electron beam) these character codes address the character generator RAM.

These character codes, when used as addresses, are combined with the three least significant line counts (L1, L2, L4) to present to the character generator output shift register all the necessary data to form an 8 element wide by 8 line high character on the CRT, located within one of the 1024 positions mentioned immediately above; that is, the 32 horizontal by 32 vertical positions.

The screen, then, is a storage place for single byte codes that call up an 8 x 8 character and place it into the corresponding character cell. This character is stored in the character generator RAM, shown on page 3 of the schematic.

3. Character Image Storage

Shown on this page are two PROMs (9C, 10C). They could be used as a permanent set of characters. However, PEPPER II™ uses RAM instead, to increase the flexibility in character manipulation. This portion of RAM appears on page 3 of the Logic schematics.

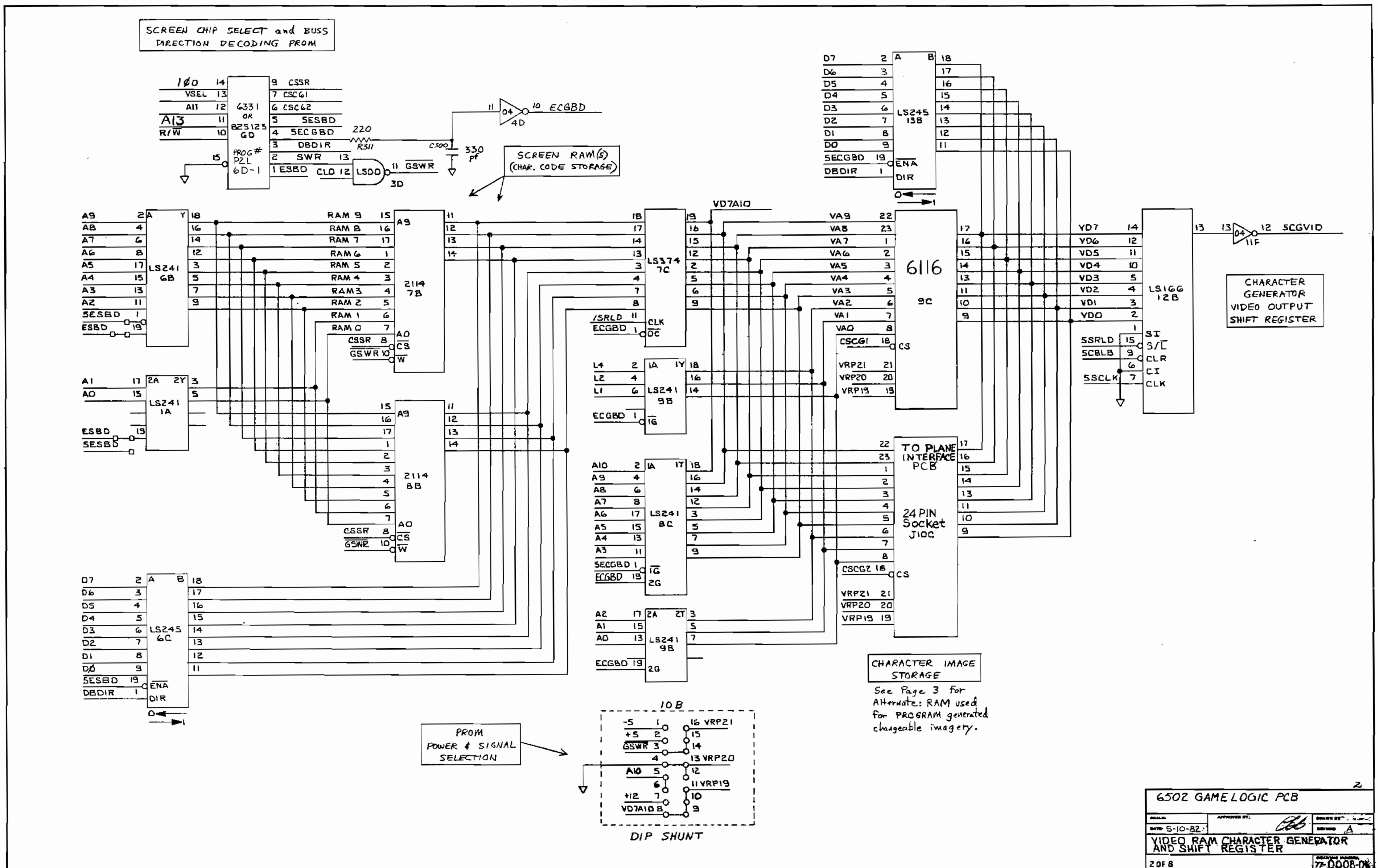
4. PROM Power and Signal Selection (10B)

This Dip Shunt configures the logic for different types of PROM devices. For PEPPER II™, however, this Dip Shunt is unnecessary due to the fact that RAM has been used rather than PROM.

5. Character Generator Output Shift Register (12B)

Video from the character generator memory devices (RAM in the case of PEPPER II™) is formed by this shift register as a byte of data that displays one line at a time from left to right on the CRT. This ultimately forms an 8 line high by 8 element wide character positioned on the screen according to the time it is presented to the shift register.

Output from this shift register are all the images seen on the screen except the player image and the player missile image.



SCREEN CHIP SELECT and BUSS DIRECTION DECODING PROM
6331 OR 82S123 6D
PROG# P2L 6D-1
SCREEN RAM(S) (CHAR. CODE STORAGE)
LS241 6B
LS241 1A
LS245 6C
2114 7B
2114 8B
LS374 7C
LS241 9B
LS241 8C
LS245 13B
6116 9C
TO PLANE INTERFACE PCB
24 PIN Socket J10C
LS166 12B
CHARACTER GENERATOR VIDEO OUTPUT SHIFT REGISTER
CHARACTER IMAGE STORAGE
See Page 3 for Alternate: RAM used for PROGRAM generated changeable imagery.
PROM POWER & SIGNAL SELECTION
10B
DIP SHUNT
ECGBD
SCGVID
VD7A10
6502 GAME LOGIC PCB
5-10-82
A
VIDEO RAM CHARACTER GENERATOR AND SHIFT REGISTER
2 OF 8
77-0008-0

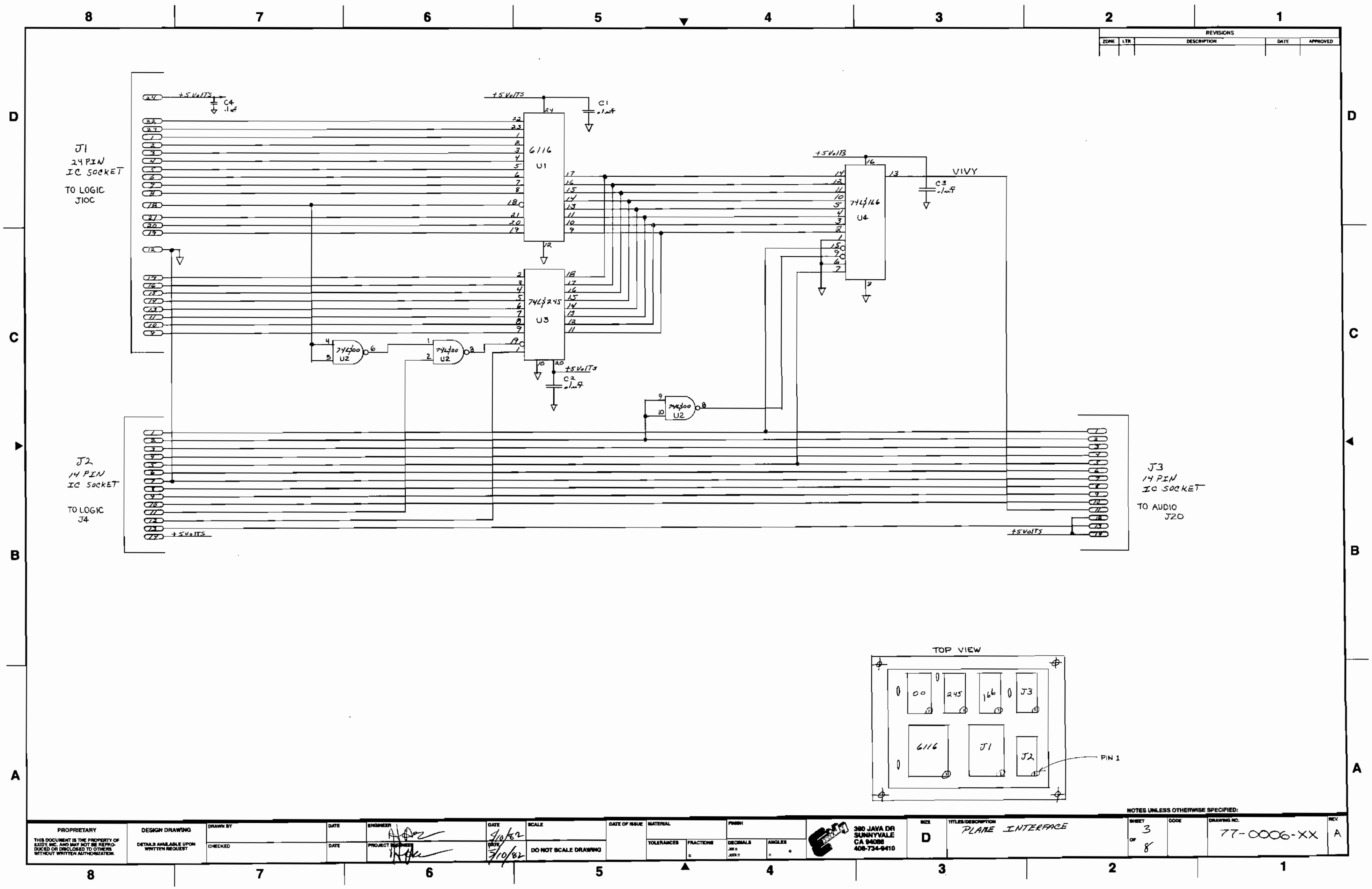
PAGE 3, PLANE INTERFACE BOARD

**Image Storage RAM**

1. Character Generator Image Storage RAM and Plane Interface Board (9C, U1)

These two RAMs, when used in this configuration, act as a 4096 x 8 bit RAM. The two color images placed on the screen are stored in this RAM by the microprocessor, according to the game program. In this RAM images are established, altered, shifted slightly, and even replaced with a new set, if required by the program.

When called by the logic to do so, the RAM presents, to the character generator shift register, a single byte, representing one line of a particular image. Each image is composed of 8 lines of data, each line is one byte-wide. Thus, 256 images of 8 x 8 bits can be stored here simultaneously and 'called up' by the screen RAM to be displayed on the CRT in any of the 1024 character cell positions. A single byte code, stored in the screen RAM, calls up a character. The character may change or move by replacing the single byte code in the screen RAM, or by altering the data in the character generator RAM which forms the image.



J1
24 PIN
IC SOCKET
TO LOGIC
J10C
J2
14 PIN
IC SOCKET
TO LOGIC
J4
J3
14 PIN
IC SOCKET
TO AUDIO
J20
+5 VOLTS
C1 .1uf
C2 .1uf
C3 .1uf
C4 .1uf
6116
U1
74LS245
U3
74LS166
U4
74LS00
U2
VIVY
TOP VIEW
00
245
166
J3
6116
J1
J2
PIN 1
REVISIONS
ZONE
LTR
DESCRIPTION
DATE
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TITLE/DESCRIPTION
PLANE INTERFACE
NOTES UNLESS OTHERWISE SPECIFIED:
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CODE
DRAWING NO.
77-0006-XX
REV.
A

## PAGE 4, GAME LOGIC PCB

### 1. The 6502 Microprocessor (2A)

For detailed information concerning this microprocessor, refer to the MOSTEK publication, 6500-10A, MCS Microcomputer Family Hardware Manual.

One feature that should be mentioned here, however, is that this microprocessor has 'memory-mapped I/O'. This means that all ports interfacing to peripherals of any type must be located within the normal memory map, with no duplication of addresses, since no instructions are specifically oriented toward I/O operations.

### 2. Power-on Reset circuit (connected to 2A pin 40)

When power is first applied to a game, a particular sequence of events must occur to set up all logic conditions. If this sequence is broken for whatever reason, the microprocessor may become confused, and the game will not start and run.

This sequence is accomplished when the reset line to the microprocessor is the last line allowed to reach a 'high' logic level. The Power-on reset circuit makes sure this occurs by utilizing the charge time of an RC network as a delay.

If any kind of power interruption occurs during normal game play, the power-on reset circuit insures that the microprocessor is reset. This alleviates confusing the microprocessor, while it also recreates the original power-on sequence.

### 3. Processor Workspace RAM (4A, 5A)

The RAM, or workspace, consists of the lowest 1024 bytes of memory and can be divided into three separate sections due to distinctly different functions.

The lowest 256 bytes (0 to FF Hexadecimal) is reserved for special software register operations, and is called 'zero page'. The processor uses this area to store dynamic variables. For details of this type of operation, refer to 6502 technical literature regarding 'Zero Page Addressing'.

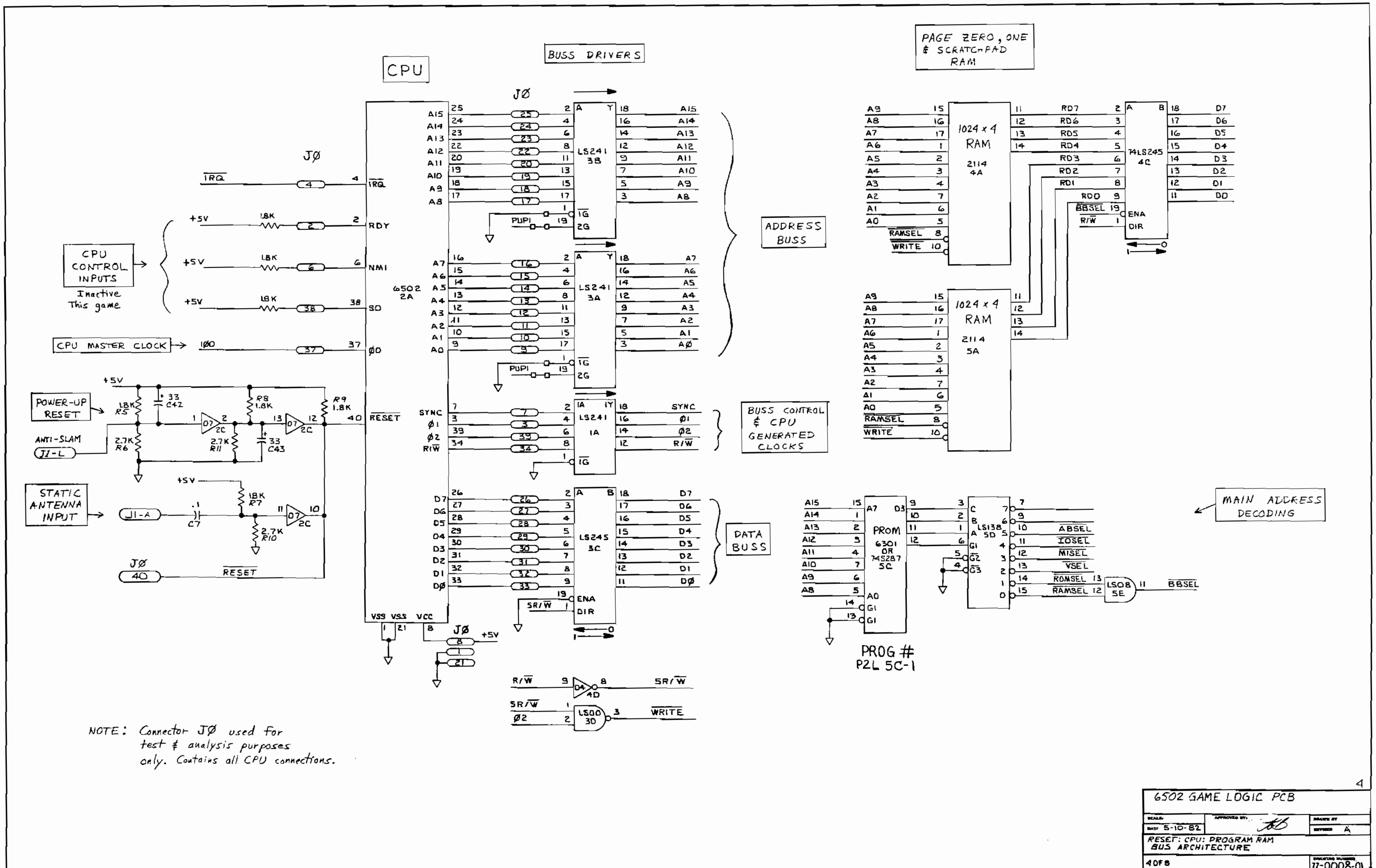
The next higher 256 bytes (100 to 1FF Hex) is reserved for the 6502 stack. The processor stores return addresses in the stack when interrupted or called to execute a subroutine. The game program may also request the processor to store other kinds of information here for later retrieval.

The next higher 512 bytes (200 to 3FF Hex) are used as a scratchpad area. Miscellaneous calculations and their results are temporarily stored here.

### 4. Main Address Decoding (5C, 5D, 5E)

This circuit is the first stage of the address line decoding necessary to organize the memory map; that is, it places specific functions or devices within generalized blocks of the memory map, grouped by function.

For details on the addressing scheme, see MEMORY MAP, Figure 1.




NOTE: Connector JØ used for test & analysis purposes only. Contains all CPU connections.

6502 GAME LOGIC PCB

DATE 5-10-82

RESET: CPU: PROGRAM RAM BUS ARCHITECTURE

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PAGE 5, GAME LOGIC PCB

1. Program Memory (6A through 13A)

These memory devices may be 2516, 2716 (5 volt only), or 2732 EPROMS. If 2516 or 2716 EPROMS are used, there will also be an additional memory expansion PCB in use to create more memory space. This PCB is simply an extension of the address, data and control lines present at the memory devices situated on the logic PCB.

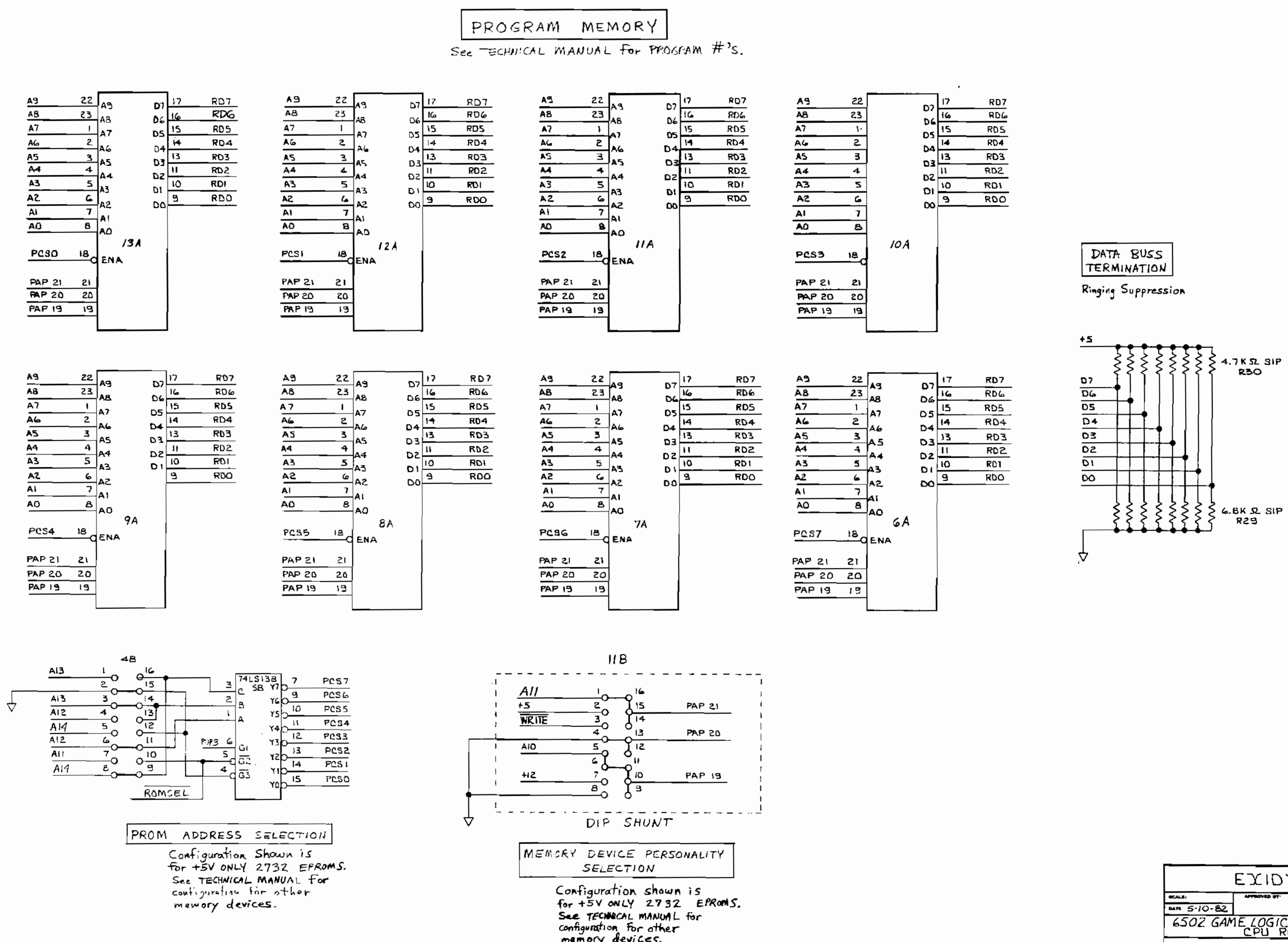
Note that four of the lines to each memory device (PCSO through PCS7, PAP19, PAP20, PAP21) are programmable through jumper configurations located at 4B and 11B. This allows different memory devices to be used and/or facilitates interconnection to the memory expansion PCB (if used).

2. PROM Address Selection (4B, 5B)

This is a second stage of address decoding, used to select each individual memory device when addressed. Signal ROMSEL (from page 4 Main Address Decoding) selects the Program Memory devices in general, and jumper 4B, together with decoder 5B further defines an address to a particular memory device.

3. Memory Device 'Personality' Selection (11B)

The dip shunt, or jumpers block, alters control signal configuration to the program memory devices. This allows the use of alternate size EPROMS and/or those created by different manufacturers whose control signal pinouts may not be identical to one another.




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REVISED A

6502 GAME LOGIC PCB CPU ROM

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5

1. Moving Object Horizontal Position (13F, 15F, 14F, 16F)

Counters 13F and 15F form a byte-wide counter which horizontally positions Moving Object 1 on the screen. These counters are preloaded to a certain value by the microprocessor during Vertical Retrace time. Then, after each occurrence of the Horizontal Sync, they begin to count. The count outputs AND'ed through 15E give rise to signal M1HW, the Horizontal Position Window for Moving Object 1. Counters 14F and 16F are the equivalent circuit for Moving Object 2.

2. Moving Object Vertical Position Counters (16E, 12E, 1E, 13E)

Counters 16E and 12E form a byte-wide counter which positions Moving Object 1 vertically on the screen. These counters are preloaded to a certain value by the microprocessor during Vertical Retrace time. Then, after each occurrence of Vertical sync, they begin counting. The four count outputs of the least significant of these two counters (M1L1, M1L2, M1L3, M1L4) are sent to the moving object image PROM to specify which line of the image is presently being displayed. The AND'ed outputs of the second counter give rise to signal M1VW, the Vertical Position Window for Moving Object 1. Counters 11E and 13E are the equivalent circuit for Moving Object 2.

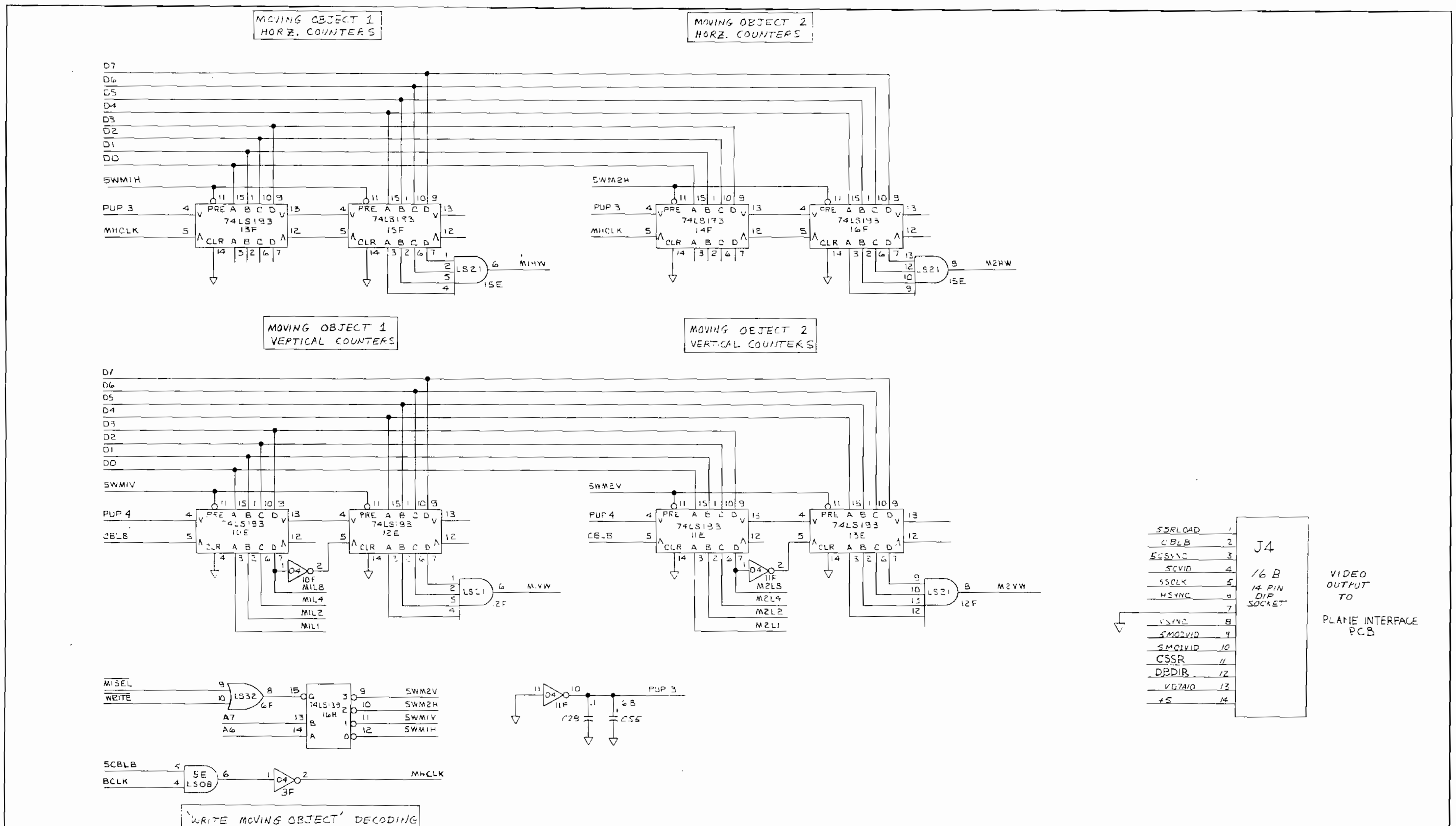
3. 'Write Moving Object' Decoding (6F, 16H, 5E, 3F)

Consists of two distinctly different functions. 6F and 16H form the circuit that generates the load pulses for the moving object position counters, while 5E and 3F simply prevent the counters from counting during blanking.

4. Color Interface Output (16B)

This is a 14 pin DIP socket used as the connector interface to the color selection circuitry, located on the audio PCB. The signals and their functions are listed below:

| Pin # | | |
|---|---|---|
| 1 | 5SRLOAD | = Shift Register Load Pulse (Neg. True) |
| 2 | CBLB | = Composite Blanking |
| 3 | CSYNC | = Composite Sync |
| 4 | 5CVID | = Composite Video (Neg. True) |
| 5 | 5SCLK | = Shift Register CLock (Neg. True) |
| 6 | HSYNC | = Horizontal Sync |
| 7 | GND | |
| 8 | VSYNC | = Vertical Sync |
| 9 | 5MO2VID | = Moving Object 2 Video (Neg. True) |
| 10 | 5MO1VID | = Moving Object 1 Video (Neg. True) |
| 11 | DBDIR | = Character Generator Address Line 9 |
| 12 | CSSR | = NOT USED ON PEPPER II |
| 13 | VD7A10 | = Character Generator Address Line 10 |
| | +5V | |




6502 GAME LOGIC PCB

COLOR INTERFACE OUTPUT AND MOVING OBJECT POSITION COUNTERS

6 OF 8

77-0008-01

1. Moving Object Multiplexing (14A, 14E)

These two multiplexers pass information to the moving objects image PROM. They contain two codes: one determines which image should appear, and the other specifies which line of that image is to be displayed.

The data passed alternates between data for Moving Object 1 and Moving Object 2, depending on the state of element count E32.

The upper multiplexer (14A) passes the 'which image' code, and the lower multiplexer (14E) passes the 'which line of that image' code.

2. Moving Objects Image PROM (11D)

This EPROM accepts as an address the image and line codes of moving objects 1 and 2 (see 'Moving Object Multiplexing' above). It then presents the appropriate data for one line of the image to the output shift registers.

The timing of the logic insures that the correct pair of shift registers are loaded with the data, then shifted out at the correct time to become, one line at a time, the 16 lines of video for that character (Moving Object 1 or 2).

3. Moving Object Video Output Shift Registers (12D, 13D, 14D, 15D)

Shift registers 12D and 13D together form a 16 bit shift register whose task is to accept, as data, 16 bits (2 bytes) representing a single line of the image for Moving Object 1, then shift these 16 parallel bits out serially to become video. This operation is repeated for 16 consecutive lines, resulting in a video image that is 16 bits wide by 16 lines high on the monitor screen.

Shift registers 14D and 15D together form this same type of circuit, identical in function, for Moving Object 2.

4. Moving Objects Shift Register Load Logic (2F, 16H)

This circuit sends properly timed load signals to the Moving Object Video Shift Registers. These load signals are needed to load the image data into the shift registers at locations 12D, 13D, 14D, and 15D.

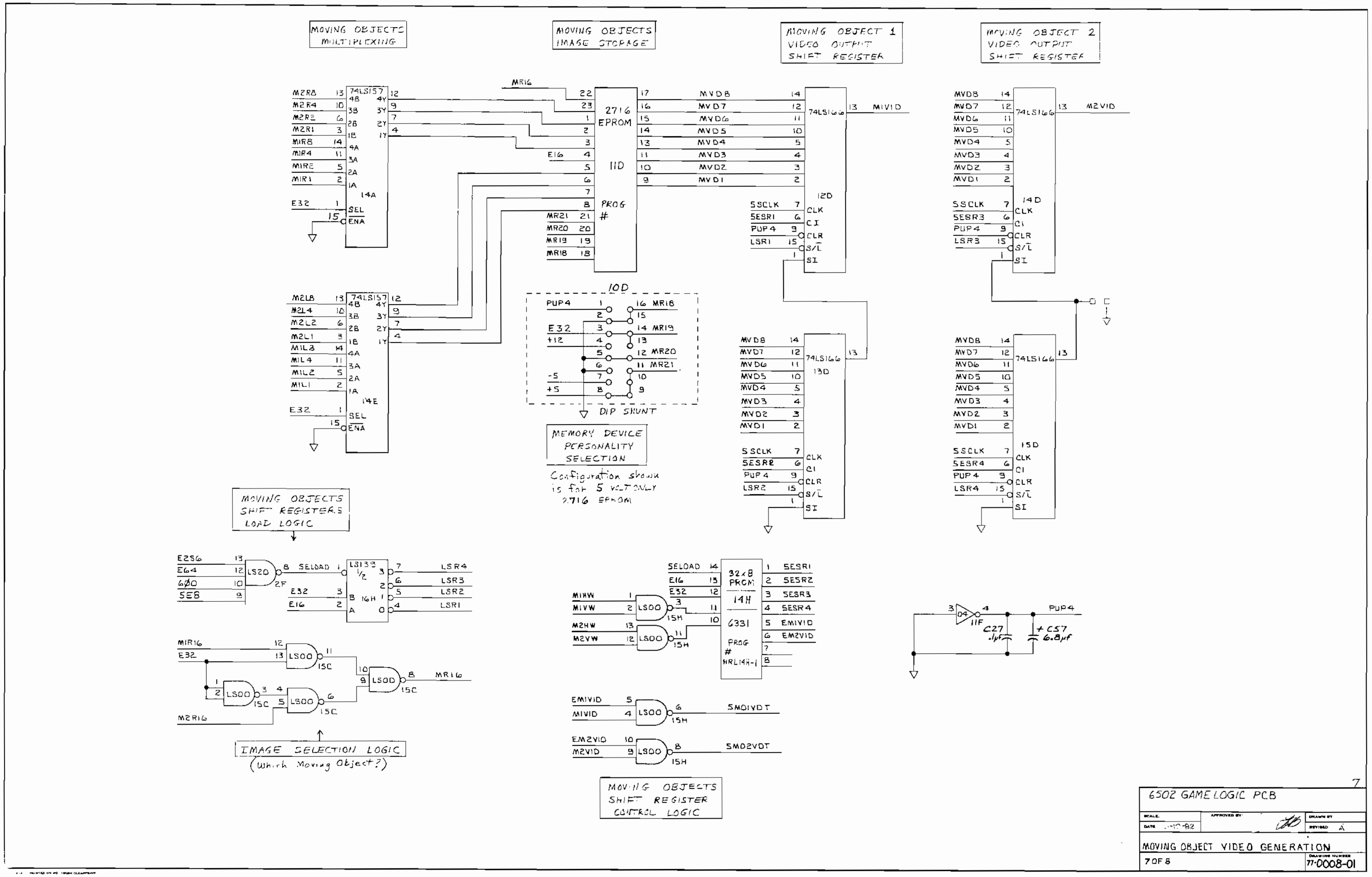
5. Moving Object Shift Register Control Logic (15H, 14H)

The input signals to the upper two gates (15H) represent horizontal and vertical position 'windows' for the two moving objects (for example, M1HW = Moving Object 1 Horizontal Window, M2VW = Moving Object 2 Vertical Window). These windows allow the Moving Object shift registers to shift only at the right time. This insures the image is generated at the correct position on the screen.

The lower 2 gates of 15H are, in PEPPER II, used for later decoding in the color selection circuitry, located on the audio PCB.

6. Memory Device Personality Configuration (10D)

This is another Dip Shunt which reconfigures the PC board in order to use an EPROM (11D) of another type or manufacturer.


MOVING OBJECTS MULTIPLEXING
MOVING OBJECTS IMAGE STORAGE
MOVING OBJECT 1 VIDEO OUTPUT SHIFT REGISTER
MOVING OBJECT 2 VIDEO OUTPUT SHIFT REGISTER
MEMORY DEVICE PERSONALITY SELECTION
Configuration shown is for 5 volt ONLY 2716 EPROM
DIP SHUNT
MOVING OBJECTS SHIFT REGISTERS LOAD LOGIC
IMAGE SELECTION LOGIC (Which Moving Object?)
MOVING OBJECTS SHIFT REGISTER CONTROL LOGIC
6502 GAME LOGIC PCB
MOVING OBJECT VIDEO GENERATION
7 OF 8
77-0008-01

1. Interrupt Status Latch (8E)

This latch is set when a coin is dropped or vertical sync occurs. When the latch is set, the CPU is interrupted; that is, signal IRQ goes low. This forces the CPU to jump to the interrupt service routine. The interrupt service routine instructs the CPU to check for a coin input, and then run a debounce routine on the coin bits of ports 9E or 15A, depending on which coin input bit was set at 8E.

If the CPU finds no coin input bit set at latch 8E, it will assume the Interrupt condition was caused by vertical sync. This tells the CPU that it should now jump to the routine that services the normal game play, and that the screen can now be updated with new data. The screen can only be updated during the vertical retrace interval.

Note that this latch also has two signals labeled LNG0 and LNG1 which both show PC etched jumpers. These two bits are the select bits for one of four languages, English, French, German, and Spanish. You may select a language by cutting the appropriate jumper, allowing it to be pulled to a logic high. For English, no cutting is necessary. See the Operator's Manual for proper configuration of other languages.

Also on this latch is the signal named TABLE. This signal, tied to a pullup resistor and switch, determines whether the program operates as a table model or in the upright game configuration. Please check with the Exidy Marketing Department and the Operator's Manual for more details, since table models may or may not be available.

2. Option Switch Port (15A)

This port provides input from the option dipswitch, at location 16A. Data from the dipswitch is gated onto the data buss and read by the CPU at game start. This allows such options as number of turns, coins per game, additional game versus extra turn, etc.

Note that one input of this port (labeled COIN 2) does not come from the switch. Instead, it comes from Coin Input 2, and is used for debouncing the auxiliary coin input switch.

3. Control Inputs Port (9E)

This port provides input from the controls located on the control panel, such as the joystick, fire button, one player start, and two player start. Data from these controls are gated onto the data buss for examination by the CPU during the regular service routine (which is synchronized to the vertical interval).

Note that one of these inputs is from the COIN1 input (labeled 5COIN1) rather than a game control input. The COIN1 input to this port is used for debouncing the standard coin input.

4. Moving Image Latch

Only the CPU can write to the moving image latch. This latch contains the code that specifies which image or images are presently being displayed by the hardware moving object circuitry.

5. Audio Board Port

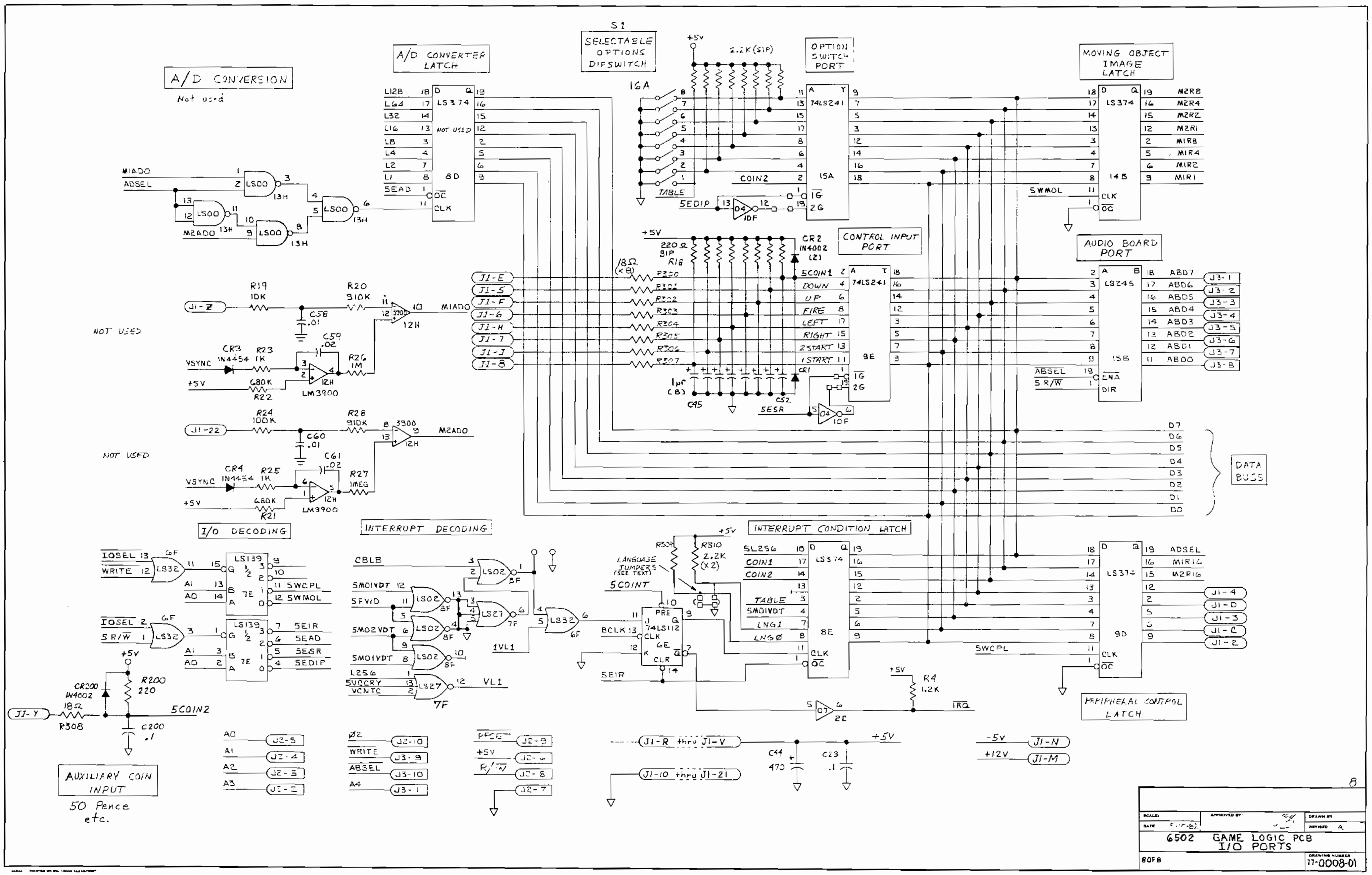
This latch is written to and read by the CPU, and transmits instructions to the audio board when any sounds are enabled, disabled, or the game is initialized. In addition, this port passes data sent to select colors for screen images. For the functions of these instructions, see the audio board schematic and/or description of operation.

6. Control Port Latch (9D)

This latch, used only in table versions, is written to only by the CPU and keeps track of which player is "up", in order to select which controls are active, that is, player one or player two.

7. I/O Decoding (7E)

The upper half of this decoder generates the chip selects for those I/O devices written to by the CPU, and the lower half generates the chip selects for those I/O devices which are read by the CPU. See the detailed memory map for more precise information.


A/D CONVERSION
Not used
A/D CONVERTER LATCH
S1 SELECTABLE OPTIONS DIPSWITCH
OPTION SWITCH PORT
MOVING OBJECT IMAGE LATCH
CONTROL INPUT PORT
AUDIO BOARD PORT
DATA BUSS
NOT USED
NOT USED
I/O DECODING
INTERRUPT DECODING
INTERRUPT CONDITION LATCH
PERIPHERAL CONTROL LATCH
AUXILIARY COIN INPUT
50 Pence etc.
6502 GAME LOGIC PCB I/O PORTS
8 OF 8
17-0008-01

## AUDIO/COLOR PCB-GENERAL DESCRIPTION

The Audio/Color PCB is so named because it contains not only the circuitry required to generate all sounds, but also the color selection decoding circuitry and video output connector.

This PCB contains a dedicated 6502 microprocessor and circuitry to support the simultaneous generation of many types of sound, including three channel music. The Logic PCB simply sends commands to the Audio/Color PCB via a bi-directional communications port and the Audio/Color PCB takes it from there. In some cases this PCB even aids the Logic PCB in some of it's calculations when there is not enough processing time available on the Logic PCB.

As a result of this structure, the actual program to generate sounds or music resides on the Audio/Color PCB. There is also a handshake required between the two PCB's in order for the system to power up correctly, and of course, there is no video output without the Audio/Color PCB connected.

PAGE 1 OF 5, AUDIO/COLOR PCB

1. Logic and Power Interface (P5,J2,J3)

Connector P5 provides the audio/color PCB with all the power it requires to operate. Also fed through this connector are the two speaker output leads. P5 interfaces only to the power supply module and the speaker, through the main harness.

Connectors J2 and J3 are the most significant path of communication between the Logic and Audio/Color PCB's. Address lines, Bi-directional Data lines, processor control lines, and the Audio/Color PCB Select line are all passed through these two connectors.

2. Communications and Address Decoding (9B,13D)

Peripheral Interface Adapter (PIA) 9B in concert with 8B (another PIA ,shown on page two) serves as a bi-directional communications path between the Logic PCB and the Audio/Color PCB. During information transfer between the two PCB's, both PIA's are in use. Information from the Logic PCB microprocessor passes through the PIA at 9B to the PIA at 8B, then to the microprocessor on the Audio/Color PCB. When information is passed the other direction, the path is the same, but the direction is reversed.

During the time that no information transfer is occurring between the two PCB's, both microprocessors can continue to operate independently.

Also shown on page one is 13D, a 3-line to 8-line decoder, used to generate the write signals for the Color Data Latches. These Latches will be covered in the text for page five of the Audio/Color PCB.

1. 6502 Microprocessor (3B)

This microprocessor is the same as that used on the Logic PCB, but is exclusively dedicated to the generation of sound. It can communicate with the Logic PCB microprocessor, and receives it's instructions thereby. Once it has received it's instructions, however, it asserts complete control over all Audio/Color PCB circuitry and ignores the Logic PCB microprocessor until such time as it is informed that another command is ready. Some commands are of a type that must be processed immediately, irregardless of other operations in progress, and some commands can wait until the operations in progress are completed. The program on the Audio/-Color PCB handles all these eventualities appropriately.

2. Peripheral Interface Adapters (8B, 7B)

The PIA at 8B, as mentioned in the text for page one, is used in bi-directional communications between the microprocessors on the Logic PCB and the Audio/Color PCB.

The PIA at 7B is used for two fundamental purposes on this PCB. The first, and most important, is that it contains the RAM that the microprocessor uses for zero page and stack operations. The PIA only contains 128 bytes of RAM, which under normal circumstances would not be sufficient for both zero page and stack. In this case, however, the memory map on this PCB has been altered, so that when the microprocessor thinks it is putting the stack at address 01FFH it is actually putting it at address 007FH.

The second use of this device is that of a programmable interval timer, used for various purposes unique to the specific sounds being generated on this game. The ability of this device to generate interrupts at time out is utilized here.

3. Address Decoding (4B)

Keyboard Encoder (4B) is used here to generate the chip selects of all devices located in the memory map of the Audio/Color PCB.

4. Music Generator (2B)

Another Programmable Counter/Timer device is used here to generate music (and sometimes other special effects) in up to three channels (or voices) simultaneously. The music is created by a special software operating system, and all but the counter/timer chip is therefore invisible.

5. Master Oscillator (A1,B1)

This oscillator is the source of all timing on the Audio/Color PCB. If this clock stops running, so does everything else on the Audio/Color PCB. It is, however, completely independent of the clock and other timing signals generated by the Master Oscillator located on the Logic PCB.

6. Program Memory (3A,4A,5A,6A,7A)

The memory devices used here are 2716 (2048 x 8) EPROMS. The DIP shunt located at 8A is used to reconfigure the control and power supply lines, if necessary, for equivalent devices from different manufacturers, whose pinouts may not be the same.

7. Output Filter Latch (1C)

This latch is used simply to switch different output filter capacitors in or out of the circuit to soften or shade the sound, according to program requirements, or to change the volume.

1. Clock Manipulation and Noise Generation Circuit (3D,4D,6D,5E)

The timers inside Programmable Timer Module 3D can be incremented or decremented either internally by the Phase Two clock input, or externally from the 'C' inputs (C1,C2,C3). Both options are used by the program. When the counters are being controlled by the Phase Two clock, the 'C' inputs have no effect, and the noise generation circuit is therefore inoperative. In order to generate sounds that are classified as noise, or contain some kind of noise within them, the counters are programmed to decrement in accordance with the input on the 'C' inputs. While in this mode, the combination of 6D (Dual 'D' Flip-Flop) and 5E (128 Bit Shift Register), are used to 'randomize' the clock inputs to the Programmable Timer Module (3D). The 'randomizer' can be clocked with either the Phase Two clock or counter output Q1.

2. Amplitude Modulation Control (2D, 7D, 8D, 9D)

Counter (3D) outputs Q1,Q2, and Q3 are already highly complex sounds, but in order to create much more specialized audio they must be modulated in amplitude. Each channel is separately controllable in amplitude by associated Digital-to-Analog converters comprised of analog multiplexers and a resistive ladder network. Three control bits on each multiplexer select a voltage to output, according to which input pin is addressed (since each input pin is tied to a different point, and therefore voltage, in the resistive ladder).

The voltage thus selected is applied to one of the two inputs to each segment of 2D (another triple analog switch). The other input is tied to ground. Note that the control bit to each analog switch segment is one of the previously mentioned count outputs (Q1,Q2,Q3). In this manner, each output can be controlled for frequency and amplitude individually.

Note also that the count output from Q1, unlike Q2 and Q3, first passes through yet another analog switch whose function is to turn off the count output of Q1 prior to reaching the Digital-to-Analog conversion stage. This is done because the Q1 output is the one used for selective clock frequency generation, and would therefore interfere with other sounds if not disabled at the appropriate time.

3. Output Summation and Special Effects Volume Control (2E)

The three segments of Operational Amplifier 2E are configured as voltage followers (for impedance considerations), and their outputs are summed together at the top of a 10K POT, R31. The output volume, therefore is determined by the voltage applied at each input and the adjustment of the POT. Note that the resistors used to sum these three outputs together are large in value, so that each channel will have minimal effect on the others when conflicting signals arrive simultaneously (except, of course, that their sum will appear at the output).

This summed output is then again summed with all other sounds generated by this PCB at the input to the final Power Amplifier.

1. Summing Amplifier and Master Volume Control (3F, R46)

One segment of Operational Amplifier 3F is used here as a point at which all the various sounds generated on this PCB are brought together. Note that the output goes immediately to a 10K POT (R46) which has ground on the other end. The wiper, therefore, varies the final output volume of all sounds together.

2. Integrator and Audio Power Amplifier (3F,10F)

Another segment of Operational Amplifier 3F is used here as an integrator; that is, it is used to 'roll off' the higher frequency sounds in order to prevent the power amplifier from going into unwanted oscillation.

The Audio Power Amplifier (10F) is a Dual Audio Amplifier IC configured as a 'Bridge Amplifier' and may be either a LM377 or LM378 for Revision A, Audio/Color PCB. Revision letters are located at position 11C. In later versions of PEPPER II it may possibly use a LM379 with a reconfigured DIP shunt.
Information regarding this is available in the operators manual for this game, or contact the Exidy Customer Service Department for assistance if you must use an alternate device.

Volume Controls

Master Volume R46, see the fourth page of Audio/Color PCB schematics.

Music Volume R9, see the fourth page of Audio/Color PCB schematics.

Special Effects Volume R3, see the fourth page of Audio/Color PCB schematics.

## PAGE 5 OF 5: AUDIO/COLOR PCB

### 1. Pattern Character Color Division (10A,9A)

The two segments of Flip-Flop 10A, using the upper two address lines from the character generator circuit, divide the character generator RAM space into four (4) conceptual groups (or quadrants) according to address. This is done in order to assign different colors to different characters.

Using this method, any character stored in a particular quadrant will be the same color as any other character stored in that same quadrant. If the same character is stored in a different quadrant, it will be displayed with a different color. The output of 9A (Two-line to Four-line decoder) applies the separated video lines of these quadrants to priority encoder 10B, whose task is to determine which image is to take visual preference when two or more coincide on the TV screen; that is, which image is to appear to be in the 'foreground', and which is to appear to be in the 'background'.

### 2. Priority Encoder (10B)

All the video signals generated by the logic PCB are applied to the priority encoder. The signals assigned the higher priority are shown at the top, and the lower priority are shown on the bottom. The output of this device is a 3 Bit code representing the highest priority video line active at that instant. This output code is then sent to the color multiplexers as an address which will select the appropriate color for the imagery generated on that video line. Note that the lowest priority input to the encoder is tied permanently low (active). This insures that when no other video is being generated, there is a background color present, unless of course, the program has selected a background color of black at that time.

### 3. Color Data Latches (11C,12C,13C)

These latches are addressed directly by the Logic PCB microprocessor. Here the microprocessor stores the data that determines which character is what color. This data is then passed to the color selection multiplexers.

### 4. Color Selection Multiplexers (11B, 12B, 13B)

Each of the three multiplexers controls the video output to a different color gun in the CRT. One turns the red gun on or off, one turns the green gun on or off, and the third does the same for the blue gun. The output combination of the three multiplexers provides for one of eight possible colors to be displayed at any given instant. The color displayed is determined by two things: what type of video is present (e.g. which character), and what color the microprocessor has currently assigned to that type of video. As mentioned above, the color assignations are stored in the color data latches. The priority encoder (10B) issues the code representing the type of video currently displayed. Using these two pieces of information, the multiplexers look at the appropriate bits in the color latches and send the data directly to the TV to turn the color guns on or off.

### 5. Video and Sync Signal Polarity Selection (11A,12A)

Before being reclocked one last time, all video outputs are passed through an Exclusive-Or gate (11A), so that one input of each segment can be used to invert the video (make it 180 degrees out of phase with respect to the input to the gate). This feature insures compatibility with TV monitors made by several different manufacturers.

The TV Sync signals are also routed through Exclusive-Or gate segments (12A) for the same purpose.

### 6. Final Video Output Re-synchronization (13A)

To insure that all video signals and sync signals are accurately synchronized in time, they are all re-clocked one last time together by a HEX 'D' Flip-Flop. It 'cleans up' any spurious irregularities or propagation delays that may have crept into any of the video or sync signals.

## PART III: ILLUSTRATED PARTS LIST FOR PEPPER II™

The following is an illustrated parts list to aid you, should you ever need to order new parts for PEPPER II™. The drawings have all parts labeled by a number within a circle. This number refers to the item number on the Parts List directly across from the drawing. In the case of the Final Assembly list, the second drawing has numbers referring to the Final Assembly list found opposite the first drawing.

Following the Illustrated Parts List is a list of parts for the Logic, Audio and Plane Interface boards.

## A. PEPPER II™ FINAL ASSEMBLY

| Item | Part Number | Description |
|---|---|---|
| 1 | D38-5137-10 | Assy, Cabinet |
| 2 | D90-0002-00 | Assy, Control Panel |
| 3 | C38-5148-10 | Assy, monitor |
| 4 | D38-5134-10 | Assy, Universal Power Supply |
| 5 | C38-5136-10 | Assy, Isolation transformer |
| 6 | 90-0035-00 | Assy, Coin Door 25 cents |
| 7 | | |
| 8 | | |
| 9 | | |
| 10 | | |
| 11 | 38-5152-10 | Assy, Flourescent Light |
| 12 | 90-0005-00 | Assy, Logic and Audio Color Board |
| 13 | C76-1225-20 | Assy, Door |
| 14 | E71-2443-10 | Assy, Main Harness |
| 15 | 71-2250-10 | Assy, Isolation Transformer Harness |
| 16 | C71-2442-10 | Assy, Speaker Harness |
| 17 | C38-5133-10 | Assy, Power Cord |
| 18 | C71-2440-10 | Ground Cable |
| 19 | B68-0035-11 | Oblong Speaker Grille |
| 20 | B68-0131-10 | lamp bracket |
| 21 | C80-0003-00 | Logo Plex |
| 22 | C75-5185-11 | Ambient shield |
| 23 | C80-0002-00 | Display Plex |
| 24 | C68-6050-20 | Coin box lid |
| 25 | C68-0124-10 | Mounting Bracket, Logo Plex Panel |
| 26 | B68-0142-10 | Hasp, Coin Box |
| 27 | C68-0141-10 | Interlock Switch Bracket |
| 28 | 83-0001-00 | Label, Serial No. Chrome/Mylar |
| 29 | B89-1019-10 | Label, Fuse |
| 30 | B89-1020-10 | Label, Voltage, 110V |
| 31 | B89-1021-10 | Label, Voltage, 220V |
| 32 | 80-0004-00 | Decal, Side art, left |
| 33 | 80-0005-00 | Decal, Side art, right |
| 34 | 70-6053 | Light, Flourescent bulb |
| 35 | 72-3000 | Switch, Interlock |
| 36 | 68-6050-10 | Coin Box, Universal |
| 37 | 74-6524 | #10-24 x 1 1/2" large carriage black |
| 38 | 74-8532 | #10-32 x 1" lg. soc. button head black |
| 39 | 74-4601 | #8 x 5/8" lg. pan hd, x-recessed type AB |
| 40 | 74-4606 | #8 x 1" lg. flat head x-recessed type AB |
| 41 | 74-5464 | #8 x 1/2" lg, sheet metal, type AB, pan head, square drive, Black |
| 42 | 74-8534 | #10-24 x 2" lg. hex hd. mach |
| 43 | 74-8544 | #10-24 x 1" lg, carriage, Blk |
| 44 | 74-5468 | #10 fender washer, 7/32" ID x 1 1/4"OD |
| 45 | 74-6513 | #10-32 kep nut |
| 46 | 74-6506 | #10-24 kep nut |
| 47 | 63-7061 | speaker |
| 48 | 88-4002 | small tywrap, 4" minature |
| 49 | 87-1001 | packing list envelope |
| 50 | 87-1062 | plastic bag, 10" x 12" |
| 51 | 00-0001-00 | Pepper Op and Service Manual |
| 52 | | |
| 53 | 33-5040 | TV Manual, Wells-Gardner #19K 4605 |
| 54 | 89-1009-10 | FCC Warning Label |
| 55 | 74-4603 | #8 X 3/4" lg, pan hd, x-rec, type AB zinc plt |
| 56 | 75-5198 | Retainer clip (flour.) |
| 57 | 74-8549 | #10-24 x 1 1/4, carriage bolt black |
| 58 | 89-1023-10 | Static Display |
| 59 | 82-1019-10 | Seal, Strain Relief Plate |
| 60 | 36-0006-00 | Plane Interface Ribbon Cable Assy |
| 61 | 36-0005-00 | Plane Interface Ribbon Cable Assy |
| 62 | 77-0006-00 | PCB Plane Interface |
| 63 | 51-6047-01 | #6 3/4", wood screw |
| 64 | 58-6070-65 | spacer, nylon 1/8" lg |
| 65 | 55-6000-01 | washer #6 flat |

## B. CONTROL PANEL ASSEMBLY 90-0002-00

| Item | Part Number | Description |
|---|---|---|
| 1 | 65-0001-00 | CONTROL PANEL FAB |
| 2 | 80-0001-00 | POLYCARBONATE OVERLAY |
| 3 | 90-0001-01 | JOYSTICK ASSY |
| 4 | B68-0140-10 | LATCH BRACKET |
| 5 | 94-0001-00 | CONTROL PANEL HARNESS ASSY |
| 7 | 74-0203 | PAL-NUT |
| 8 | 72-3062-11 | PUSH BUTTON |
| 9 | 72-3061-11 | SWITCH ASSY |
| 10 | 74-5247 | 10-24 X 5/8" CARRIAGE BOLT, BLK.ZN |
| 11 | 53-0042-01 | 10-24 NYLOCK NUT |
| 12 | 74-8548 | #6-32 X 3/8" LARGE FLAT HEAD, X-REC., MACHINE ZINC PLATE |

European Version:

| | | |
|---|---|---|
| | 90-0001-02 | JOYSTICK ASSY |
| | 94-0002-00 | CONTROL PANEL HARNESS ASSEMBLY |

C. JOYSTICK (90-0001-00)

(Part Numbers included on drawing, opposite this page)

## D. UNIVERSAL POWER SUPPLY ASSEMBLY, 90-0006-00

| Item | Part Number | Description |
|---|---|---|
| 1 | C76-1258-10 | POWER SUPPLY MOUNTING BOARD |
| 2 | 74-3503 | SCREW, PAN HD, #6 X 1/2" LG. TYPE AB |
| 3 | 74-2516 | SPACER, #6 x .125 NON-METALLIC |
| 4 | 74-5198 | SCREW, PAN HD. #6-32 x 3/4" LG. |
| 5 | 74-3500 | WASHER, FLAT, #6 |
| 6 | 74-3502 | NUT, KEP, #6-32 |
| 7 | 78-3001 | POWER SUPPLY, 5V @ 6.0 AMPS |
| 8 | 63-4028 | TRANSFORMER, FILAMENT, 24V @ 4.0 AMPS |
| 9 | 77-0009-05 | PRINTED CIRCUIT ASSEMBLY UNIVERSAL POWER SUPPLY |
| 10 | C71-2389-10 | HARNESS, POWER SUPPLY |
| 11 | 71-2255-10 | HARNESS, POWER SUPPLY FLOURESCENT |
| 12 | 80-4004 | 1/4" SHRINK TUBING |
| 13 | 88-4002 | TYRAP |

## E. ISOLATION TRANSFORMER ASSEMBLY, C38-5136-10

| Item | Part Number | Description |
|---|---|---|
| 1 | 63-4029 | TRANSFORMER, ISOLATION |
| 2 | B76-1259-10 | BOARD MTG. TRANS |
| 3 | 74-5463 | SCREW, PAN HD. #10-24 X 1.00' LG |
| 4 | 74-5468 | WASHER, FENDER, #10 |
| 5 | 74-6402 | WASHER, FLAT, #10 |
| 6 | 74-6506 | NUT, KEP, #10-24 |
| 7 | 61-8058 | 3 PIN MOLEX PLUG |
| 8 | 61-8055 | FEMALE MOLEX PINS |
| 9 | 61-8357 | 2 PIN MOLEX RECEPTACLE |
| 10 | | WIRE, COPPER, STRANDED #18 AWG |
| 11 | 74-8536 | TERMINAL, RING #10 STUD |
| 12 | 61-8072 | SPLICE, BUTT |
| 13 | 61-8054 | MALE MOLEX PIN |

## F. COIN DOOR ASSEMBLY, 90-0003-00

| Item | Part Number | Description |
|---|---|---|
| 1 | 90-0032-00 | COIN DOOR, MODIFIED |
| 2 | 90-0031-00 | COIN ACCEPTOR- MODIFIED |
| 3 | 74-3502 | NUT-KEP #6-32 |
| 4 | 71-2444-10 | UNIVERSAL COIN HARNESS ASSY |

## G. LOGIC AND AUDIO BOARD ASSEMBLY 90-0005-00

| | | |
|---|---|---|
| 1 | 77-0008-05 | PWA LOGIC |
| 2 | 77-0007-05 | PWA AUDIO COLOR |
| 3 | 74-8552 | SPACER NON-METALLIC #6-32 X 7/8 LONG |
| 4 | 74-5182 | SCREW, PAN HD. PHIL #6-32 x 1/4 LG |
| 5 | 36-0006-00 | CABLE ASSY, RIBBON, 14 PIN |
| 6 | 74-5173 | WASHER, FLAT, NYLON #6 |
| 7 | 36-0005-00 | PLANE INTERFACE RIBBON CABLE |
| 8 | 77-0006-05 | PLANE INTERFACE PCB ASSEMBLY |

## H. PRINTED CIRCUIT ASSEMBLY-UNIVERSAL POWER SUPPLY, 77-0009-05

| | | |
|---|---|---|
| 1 | 77-0009-04 | UNIVERSAL POWER SUPPLY BOARD |
| 2 | 13-4085-00 | CAP, ELECT. 4000MF, 50V AXIAL LEAD |
| 3 | 13-3364-00 | CAP, ELECT. DIP 33MF 25V + 20% |
| 4 | 13-6844-0 | CAP, ELECT. DIP 6.8MF 25V + 20% |
| 5 | 20-0003-00 | DIODE 60S1 or UT4010 |
| 6 | 20-0005-00 | RECTIFIER, BRIDGE MDA-970-1 |
| 7 | 21-0003-00 | TRANSISTOR, 2N3055 |
| 8 | 21-0004-00 | TRANSISTOR, 2N6246 |
| 9 | 21-0005-00 | REGULATOR 7905 |
| 10 | 21-0006-00 | REGULATOR 7912 |
| 11 | 84-0012-00 | HEATSINK |
| 12 | 84-0013-00 | HEATSINK |
| 13 | 40-0002-00 | CONNECTOR 12 PIN (WAFER HEADER) |
| 14 | 50-4027-00 | SCREW, PAN HD #4-40 x 3/8 LG (PHIL) |
| 15 | 53-4011-01 | NUT, KEP #4-40 |
| 16 | 37-0001-00 | TYRAP 5 1/2" |

## I. LOGIC BOARD, 77-0008-05

| Item | Part Number | Description | Location |
|---|---|---|---|
| 1 | 77-0008-04 | PCB LOGIC | |
| 2 | 22-0001-02 | I.C. 74LS00 | 3D, 15C, 15H |
| 3 | 22-0002-02 | I.C. 74LS02 | 1H, 6H, 8F |
| 4 | 22-0003-02 | I.C. 74LS04 | 1D, 4D, 3F, 10F, 11F |
| 5 | 22-0004-00 | I.C. 7407 | 2C |
| 6 | 22-0005-02 | I.C. 74LS08 | 5E |
| 7 | 22-0006-02 | I.C. 74LS11 | 3H |
| 8 | 22-0007-02 | I.C. 74LS20 | 2F |
| 9 | 22-0008-02 | I.C. 74LS21 | 12F, 15E |
| 10 | 22-0009-02 | I.C. 74LS27 | 7F, 2H |
| 11 | 22-0010-02 | I.C. 74LS32 | 6F |
| 12 | 22-0011-02 | I.C. 74LS74 | 1C |
| 13 | 22-0012-02 | I.C. 74LS112 | 2E, 6E |
| 14 | 22-0013-02 | I.C. 74LS138 | 5B, 5D |
| 15 | 22-0014-02 | I.C. 74LS139 | 7E, 16H |
| 16 | 22-0015-02 | I.C. 74LS157 | 14A, 14E |
| 17 | 22-0016-02 | I.C. 74LS161 | 1E, 2D, 4F, 5F |
| 18 | 22-0017-02 | I.C. 74LS166 | 12B, 12D, 13D, 14D, 15D |
| 19 | 22-0018-02 | I.C. 74LS193 | 10E, 12E, 13F, 15F, 14FM 16F, 11E 13E |
| 20 | 22-0019-02 | I.C. 74LS241 | 1A, 3A, 15A, 3B, 6B, 9B, 8C, 7D, 9E, 4H |
| 21 | 22-0020-02 | I.C. 74LS245 | 3C, 4C, 6C, 13B, 15B |
| 22 | 22-0021-02 | I.C. 74LS374 | 1F, 14B, 7C, 9D, 8E |
| 23 | 25-0004-00 | MICROPROCESSOR 6502 | 2A |
| 24 | 28-0004-00 | 2114 RAM (1K x 4) | 4A, 5A, 7B, 8B |
| 25 | 24-0011-00 | 6301 PROM (256x4) P2L5C-1 | 5C |
| 26 | 24-0012-00 | 6331 PROM (32x8) P2L6D-1 | 6D |
| 27 | 24-0013-00 | 6331 PROM (32x8) HRL14H-1 | 14H |
| 28 | 20-0001-01 | 1N4002 DIODE | 8E, 9F, 2H |
| 29 | 02-4712-00 | RES. 470 OHM 1/4W 5% | 1D, 2H |
| 30 | 02-1222-00 | RES. 1.2K 1/4W 5% | 2C |
| 31 | 02-1822-00 | RES. 1.8K 1/4W 5% | 1C, 2C |
| 32 | 02-2222-00 | RES. 2.2K 1/4W 5% | 7E, 2A |
| 33 | 02-2722-00 | RES. 2.7K 1/4W 5% | 1C, 2C |
| 34 | 09-0007-00 | RES. 220 OHM 1/8W 5% 10 Pin Sip | 9E |
| 35 | 09-0004-00 | RES. 2.2K 1/8W 5% 10 Pin Sip | |
| 36 | 09-0008-00 | RES. 4.7K 1/8W 5% 10 Pin Sip | 15A |
| 37 | 09-0009-00 | RES. 6.8K 1/8W 5% 10 Pin Sip | 14A |
| 38 | 23-0045-00 | CAP. .01uf CERAMIC DISC | 1D |
| 39 | 10-1034-1 | CAP. .1uf CERAMIC DISC | A/R |

## I. LOGIC BOARD, continued

| Item | Part Number | Description | Location |
|---|---|---|---|
| 40 | 10-1044-1 | CAP. 6.8uf 25v DIPTANT | 1C, 15D, 6E, 13F |
| 41 | 13-6844-1 | CAP. 33uf 25V ELECTROLYTIC | 1C, 2C |
| 42 | 13-3365-0 | CAP. 470uf 10V ELECTROLYTIC | 10H |
| 43 | 13-4775-0 | DIPSHUNT JUMPER PAKS 16 PIN | 4B, 11B, 10D |
| 44 | 47-0001-00 | DIP SWITCH 8 POS. | 16A |
| 45 | 49-5002-00 | CRYSTAL 11.289mhz (SERIES) | 1D |
| 46 | 29-0001-00 | 10 PIN MALE MOLEX HDR | 16C, 16F |
| 47 | 40-0061-00 | DIP SOCKETS 16 PIN LOW PROFILE | 4B, 11B, 5C, 6D 14H, 10D |
| 48 | 44-1601-00 | DIP SOCKETS 24 PIN LOW PROFILE | 6A thru 13A, 11D |
| 49 | 44-2401-00 | DIP SOCKETS 40 PIN LOW PROFILE | 2A |
| 50 | 44-4001-00 | DIP SOCKETS 14 PIN LOW PROFILE | 16B |
| 51 | 44-1401-00 | DIP SOCKETS 18 PIN LOW PROFLE | 4A, 5A, 7B, 8B, 11C 12C, 13C, 14C |
| 52 | 44-1801-00 | CAP 1uf DIPTANT | C45 thru C52, 5D, 2H |
| 53 | 11-1053-00 | RES. 220 OHM 1/4W 5% | R200, R311 |
| 54 | 02-2212-00 | RES. 18 OHM 1/4W 5% | R300 thru R302 |
| 55 | 02-1802-00 | CAP. 330 pf CER. DISC | 5D |
| 56 | 23-0050-03 | E PROM, 2732 P2L6A-1 | 6A |
| 57 | 23-0051-03 | E PROM, 2732 P2L7A-1 | 7A |
| 58 | 23-0052-03 | E PROM, 2732 P2L8A-1 | 8A |
| 59 | 23-0053-03 | E PROM, 2732 P2L9A-1 | 9A |
| 60 | 10-2214-4 | CAP 220 pf CERAMIC DISC | |
| 61 | 23-0054-03 | E PROM, 2732 P2L10A-1 | 10A |
| 62 | 23-0055-03 | E PROM, 2732 P2L11A-1 | 11A |
| 63 | 23-0056-03 | E PROM, 2732 P2L12A-1 | 12A |
| 64 | 23-0049-00 | E PROM, 2716 P2L11D-1 | 11D |

## J. AUDIO/COLOR BOARD ASSEMBLY 77-0007-05

| | | | |
|---|---|---|---|
| 1 | 77-0007-04 | PRINTED CIRCUIT BOARD | |
| 2 | 22-0013-02 | I.C. 74LS138 | 13D |
| 3 | 26-0003-00 | I.C. 6520 | 8B, 9B |
| 4 | 25-0002-00 | I.C. 6532 | 7B |
| 5 | 25-0004-00 | I.C. 6502 | 3B |
| 6 | 27-0001-00 | I.C. 6840 | 3D |
| 7 | 22-0022-02 | I.C. 74LS154 | 4B |
| 8 | 27-0002-00 | I.C. 8253 | 2B |
| 9 | 22-0023-00 | I.C. 4069 | 1A |
| 10 | 22-0055-00 | I.C. 4013B | 1B |

## J. AUDIO/COLOR BOARD ASSEMBLY, continued

| Item | Part Number | Description | Location |
|---|---|---|---|
| 11 | 22-0003-02 | I.C. 74LS04 | 5D |
| 12 | 22-0001-02 | I.C. 74LS00 | 6B |
| 13 | 22-0021-02 | I.C. 74LS374 | 1C, 11C, 12C, 13C |
| 14 | 22-0024-00 | I.C. 4053 | 2D, 4D |
| 15 | 22-0025-00 | I.C. 4175 | 6E, 73, 8E, 9E |
| 16 | 22-0056-00 | I.C. 4562 | 5E |
| 17 | 22-0011-02 | I.C. 74LS74 | 10A, 6D |
| 18 | 22-0026-00 | I.C. LM324 | 3F, 2E |
| 19 | 22-0054-00 | I.C. 7406 | 1D |
| 20 | 22-0027-02 | I.C. 74LS86 | 11A, 12A, 4E |
| 21 | 22-0028-00 | I.C. 4051 | 7D, 8D, 9D |
| 22 | 22-0014-02 | I.C. 74LS139 | 9A |
| 23 | 22-0057-00 | I.C. LM377 | 10E |
| 24 | 22-0029-02 | I.C. 74LS148 | 10B |
| 25 | 22-0030-02 | I.C. 74LS151 | 11B, 12B, 13B |
| 26 | 22-0031-02 | I.C. 74LS174 | 13A |
| 27 | 10-1044-1 | .1 uf. CERAMIC CAP 25V | 1A thru 7A, 9A, 11A, 13A, 1B, 6B, 9B, 11B, 1C, 11C, 13C, 1D 3D, 5D, 7D, 9D, 11D, 13D, 1E, 2E, C7, C9, C10, 3E, 5E, 7E, 9E, C12, 13E, 2F, 4F, 12F, 9E, 2E, 3F |
| 28 | 10-2204-1 | 22pf CERAMIC CAP 16V. | C1 |
| 29 | 10-1034-1 | .01 uf CERAMIC CAP 16V | C6, C8, C11, C33, 1C |
| 30 | 13-3365-1 | 33uf CAP, 25V, ELECTROLYTIC W/AXIAL LEADS | C13, C15, C17 thru C21 |
| 31 | 13-1075-00 | 100uf CAP ELECTRO-LYTIC 16V | C16 |
| 32 | 13-4755-00 | 4.7uf CAP ELECTRO-LYTIC 16V | C3, C4, C5 |
| 33 | 13-1055-00 | 1.0uf CAP ELECTRO-LYTIC 16V | C27, C32, C2 |
| 34 | 02-1822-00 | 1.8K RES. 1/4W 5% | R3, R4, R5 |
| 35 | 02-3322-00 | 3.3K RES. 1/4W 5% | R6 |
| 36 | 02-1022-00 | 1K RES. 1/4W 5% | R14 |
| 37 | 02-1062-00 | 10M RES. 1/4W 5% | R2 |
| 38 | 02-3012-00 | 300 OHM RES. 1/4W 5% | R1 |
| 39 | 02-1042-00 | 100K RES. 1/4W 5% | R10, R11, R12, R27 R47, 428, R29 |
| 40 | 02-2232-00 | 22K RES. 1/4W 5% | R15, R30 |
| 41 | 02-1052-00 | 1M RES. 1/4W 5% | R32 R33, R35 |
| 42 | 02-3332-00 | 33K RES. 1/4W 5% | R34 |
| 43 | 02-2722-00 | 2.7K RES. 1/4W 5% | R21 |
| 44 | 02-2732-00 | 27K RES. 1/4W 5% | R44 |
| 45 | 02-1322-00 | 1.3K RES. 1/4W 5% | R26 |
| 46 | 02-6812-00 | 680 OHM RES. 1/4W 5% | R19 |
| 47 | 02-3312-00 | 330 OHM RES. 1/4W 5% | R7, R8, R24 |
| 48 | 02-1612-00 | 160 OHM RES. 1/4W 5% | R25 |

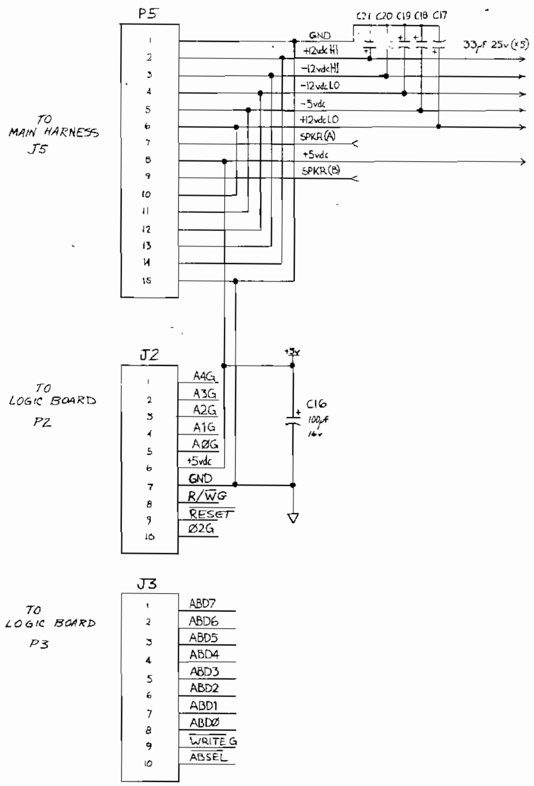
J. AUDIO/COLOR BOARD ASSEMBLY, continued

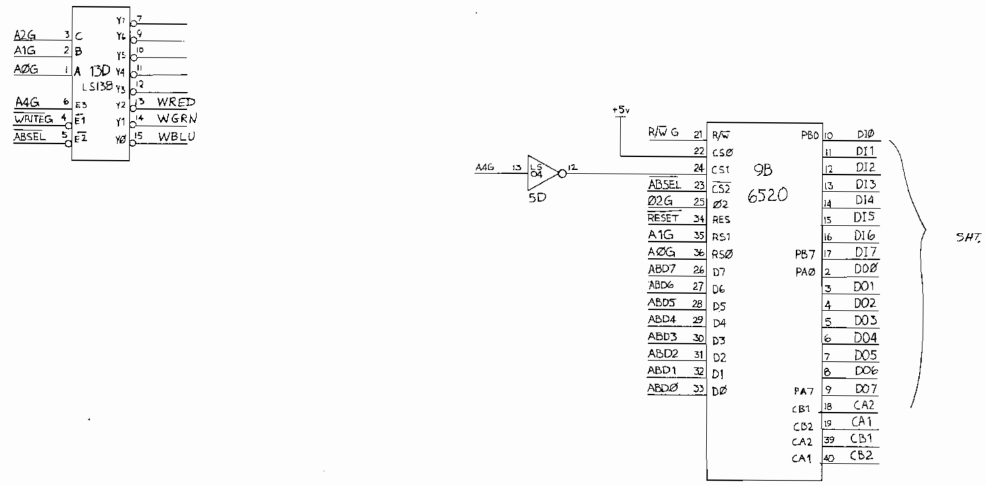
| Item | Part Number | Description | Location |
|---|---|---|---|
| 49 | 02-8202-00 | 82 OHM RES. 1/4W 5% | R20 |
| 50 | 02-3902-00 | 39 OHM RES. 1/4W 5% | R22, R23 |
| 51 | 07-1032-00 | 10K RES. 1/4W 5% | R16, R17, R18, R42, R45 |
| 52 | 07-0004-00 | 10K POT | R9, R31, R46 |
| 53 | 09-0008-00 | 4.7K RES. PAC 10 PIN SIP | 4D |
| 54 | 29-0002-00 | 3.579545 MHZ CRYSTAL | 2A |
| 55 | 47-0001-00 | 16 PIN DIP SHUNT | 8A, 11E |
| 56 | 44-1401-00 | 14 PIN DIP SOCKET | J20, 1A, 1B, 5E |
| 57 | 44-2401-00 | 24 PIN DIP SOCKET | 3A, 4A, 5A, 6A, 7A, 2B |
| 58 | 44-2801-00 | 28 PIN DIP SOCKET | 3D |
| 59 | 44-4001-00 | 40 PIN DIP SOCKET | 3B, 7B, 8B, 9B |
| 60 | 44-1601-00 | 16 PIN DIP SOCKET | 2D, 4D, 8A, 11E, 6E- 9E, 7D-9D |
| 61 | 13-4735-00 | .47 uf CAP ELECTRO-LYTIC 16V | C14 |
| 62 | 40-0005-10 | 10 PIN MALE CONNECTOR | P21 |
| 63 | 37-0009-00 | 10 PIN FLAT CABLE ASSEMBLY | J2, J3 |
| 64 | 75-0006-00 | HEATSINK STAVER V7-1 | ONLY W/ LM277, LM278 |
| 65 | 23-0048-00 | E PROM 2716, P2A3A-1 | 5A |
| 66 | 23-0047-00 | E PROM 2716, P2A4A-1 | 6A |
| 67 | 23-0046-00 | E PROM 2716, P2A5A-1 | 7A |
| 68 | 41-0003-00 | FEMALE 10 PIN | |

K. PLANE INTERFACE BOARD 77-0006-05

| Part Number | Description |
|---|---|
| 77-0006-04 | PLANE INTERFACE BOARD |
| 10-1044-1 | .1UF CAP., 25 VOLT |
| 22-0001-02 | I.C. 74LS00 |
| 22-0017-02 | I.C., 74LS166 |
| 22-0020-02 | I.C. 74LS245 |
| 23-0045-00 | I.C., 6116 |
| 44-1401-00 | 14 PIN SOCKET |
| 44-2401-00 | 24 PIN SOCKET |

| REV | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|
| | PRODUCTION RELEASE | 6-0-82 | |




NOTE:
ALL RESISTORS ARE 1/4 WATT, 5%.
ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

BYPASS .1μf FOR EVERY OTHER I.C.

THIS TABLE REFERS TO POWER & GND PINS NOT SCHEMATICALLY REPRESENTED.

| DEVICE TYPE | +5v | GND |
|---|---|---|
| 6520 | 20 | 1 |
| 4069 | 14 | 7 |
| 4013 | 14 | 7 |
| 6502 | 8 | 1,21 |
| 6532 | 20 | 1 |
| LS154 | 24 | 12 |
| 8253 | 24 | 12 |
| LS00 | 14 | 7 |
| LS374 | 20 | 10 |
| LS138 | 16 | 8 |
| LS86 | 14 | 7 |
| LS139 | 16 | 8 |
| 4175 | 16 | 8 |
| 4053 | 16 | 8 |
| LS74 | 14 | 7 |
| LS04 | 14 | 7 |
| 7406 | 14 | 7 |
| 4175 | 16 | 8 |
| 4051 | 16 | 8 |
| 4562 | 14 | 7 |
| 74151 | 16 | 8 |
| 74148 | 16 | 8 |
| LS174 | 16 | 8 |

13

NOTES UNLESS OTHERWISE SPECIFIED

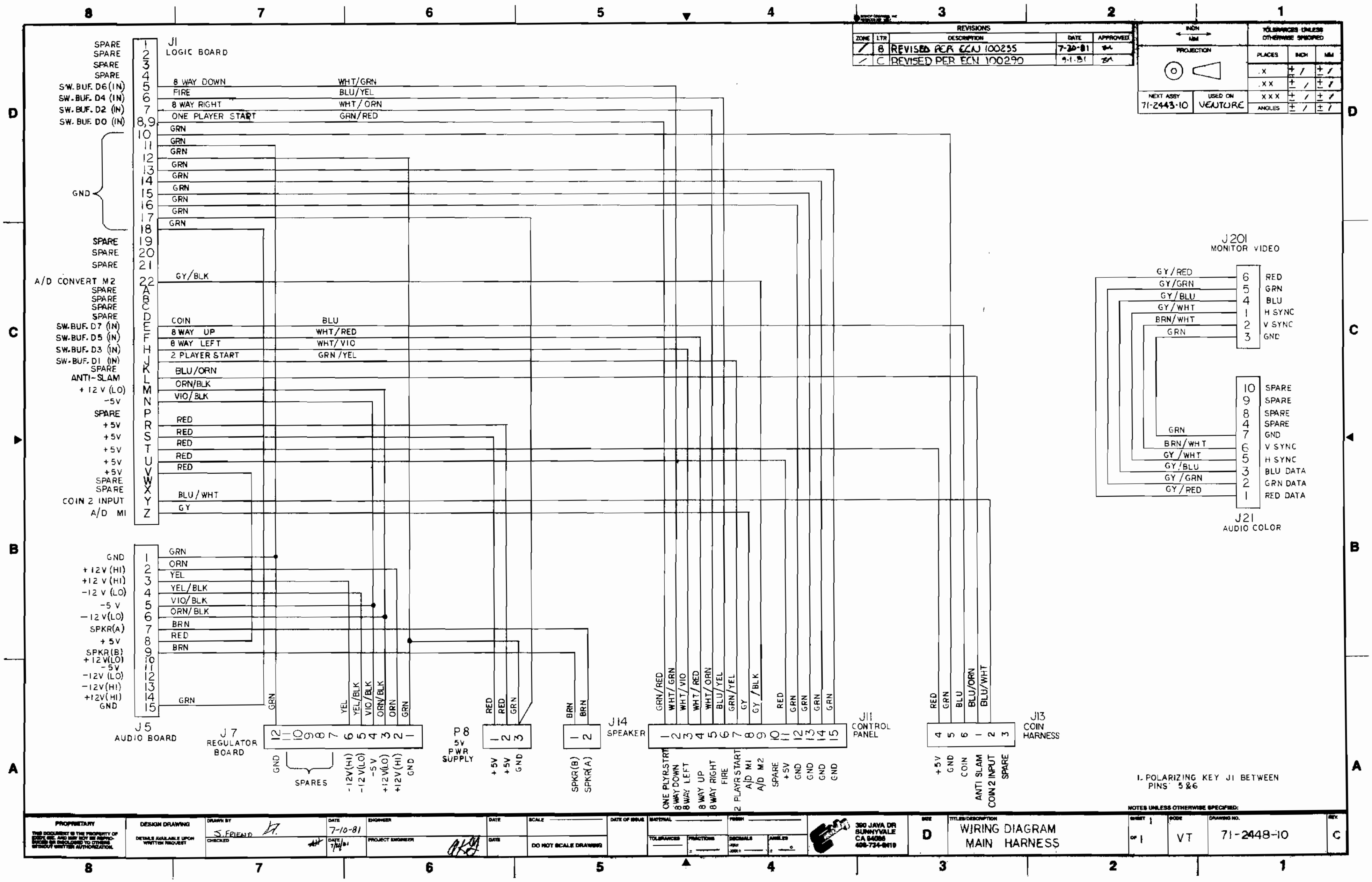


DESIGN DRAWING
DETAILS AVAILABLE UPON WRITTEN REQUEST

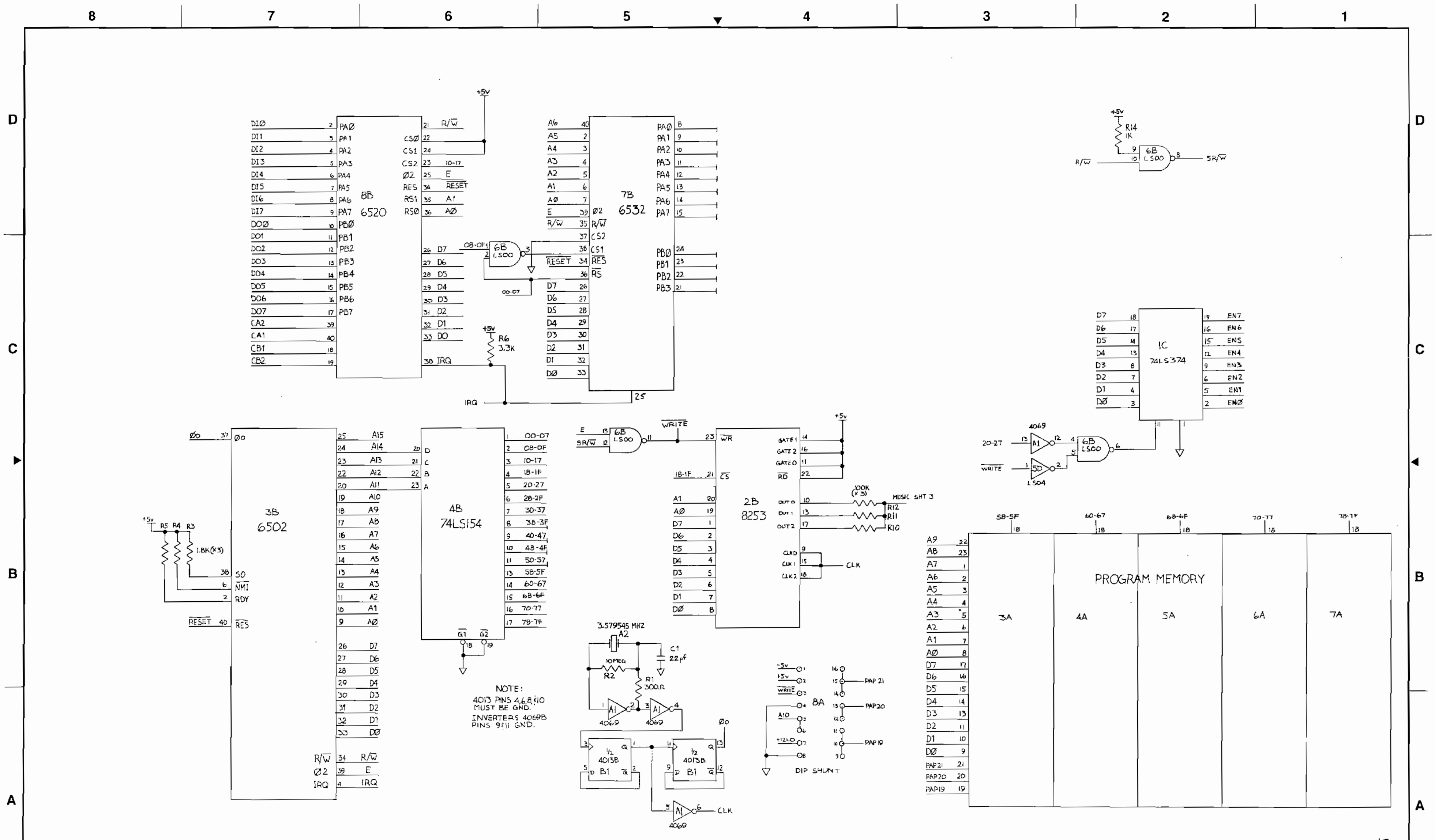
DRAWN BY: NEAL R. ZOOK — DATE: 6-8-81
ENGINEER: MARK VON STRIVER — DATE: 6-8-81
DO NOT SCALE DRAWING

390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

SIZE: D
TITLE/DESCRIPTION: AUDIO/COLOR PCB SCHEMATIC DIAGRAM
SHEET 1 OF 5
DRAWING NO: 77-0007-01
REV: A



J1 LOGIC BOARD
SPARE
SPARE
SPARE
SPARE
SW. BUF. D6 (IN)
SW. BUF. D4 (IN)
SW. BUF. D2 (IN)
SW. BUF. D0 (IN)
GND
SPARE
SPARE
SPARE
A/D CONVERT M2
SW. BUF. D7 (IN)
SW. BUF. D5 (IN)
SW. BUF. D3 (IN)
SW. BUF. D1 (IN)
ANTI-SLAM
+12 V (LO)
-5V
+5V
COIN 2 INPUT
A/D MI
8 WAY DOWN
FIRE
8 WAY RIGHT
ONE PLAYER START
COIN
8 WAY UP
8 WAY LEFT
2 PLAYER START
WHT/GRN
BLU/YEL
WHT/ORN
GRN/RED
GRN
GY/BLK
BLU
WHT/RED
WHT/VIO
GRN/YEL
BLU/ORN
ORN/BLK
VIO/BLK
RED
BLU/WHT
GY
J5 AUDIO BOARD
GND
+12V (HI)
-12 V (LO)
-5 V
-12 V(LO)
SPKR(A)
+5 V
SPKR(B)
+12V(LO)
-12V (LO)
-12V(HI)
+12V(HI)
ORN
YEL
YEL/BLK
VIO/BLK
ORN/BLK
BRN
J7 REGULATOR BOARD
SPARES
-12V(HI)
-12V(LO)
+12V(LO)
+12V(HI)
P8 5V PWR SUPPLY
J14 SPEAKER
SPKR(B)
SPKR(A)
J11 CONTROL PANEL
ONE PLYR.STRT
8 WAY DOWN
8 WAY LEFT
8 WAY UP
8 WAY RIGHT
2 PLAYR START
A/D M1
A/D M2
SPARE
J13 COIN HARNESS
ANTI SLAM
COIN 2 INPUT
J201 MONITOR VIDEO
GY/RED
GY/GRN
GY/BLU
GY/WHT
BRN/WHT
H SYNC
V SYNC
J21 AUDIO COLOR
BLU DATA
GRN DATA
RED DATA
1. POLARIZING KEY J1 BETWEEN PINS 5 & 6
NOTES UNLESS OTHERWISE SPECIFIED:
REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
B REVISED PER ECN 100235 7-20-81
C REVISED PER ECN 100290 9-1-81
PROJECTION
NEXT ASSY 71-2443-10
USED ON VENTURE
TOLERANCES UNLESS OTHERWISE SPECIFIED
PLACES
INCH
MM
ANGLES
PROPRIETARY
DESIGN DRAWING
DETAILS AVAILABLE UPON WRITTEN REQUEST
DRAWN BY S. FRIEND
DATE 7-10-81
CHECKED
DO NOT SCALE DRAWING
390 JAVA DR SUNNYVALE CA 94086 408-734-8410
SIZE D
TITLE/DESCRIPTION WIRING DIAGRAM MAIN HARNESS
SHEET 1 OF 1
CODE VT
DRAWING NO. 71-2448-10
REV C




PROPRIETARY

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DESIGN DRAWING

DETAILS AVAILABLE UPON WRITTEN REQUEST

| DRAWN BY | DATE | ENGINEER | DATE | SCALE |
|---|---|---|---|---|
| NEAL R ZOOK | 6-5-81 | MARK VON STRIVER | 6-6-81 | |
| CHECKED | DATE | PROJECT ENGINEER | DATE | DO NOT SCALE DRAWING |

390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

NOTES UNLESS OTHERWISE SPECIFIED:

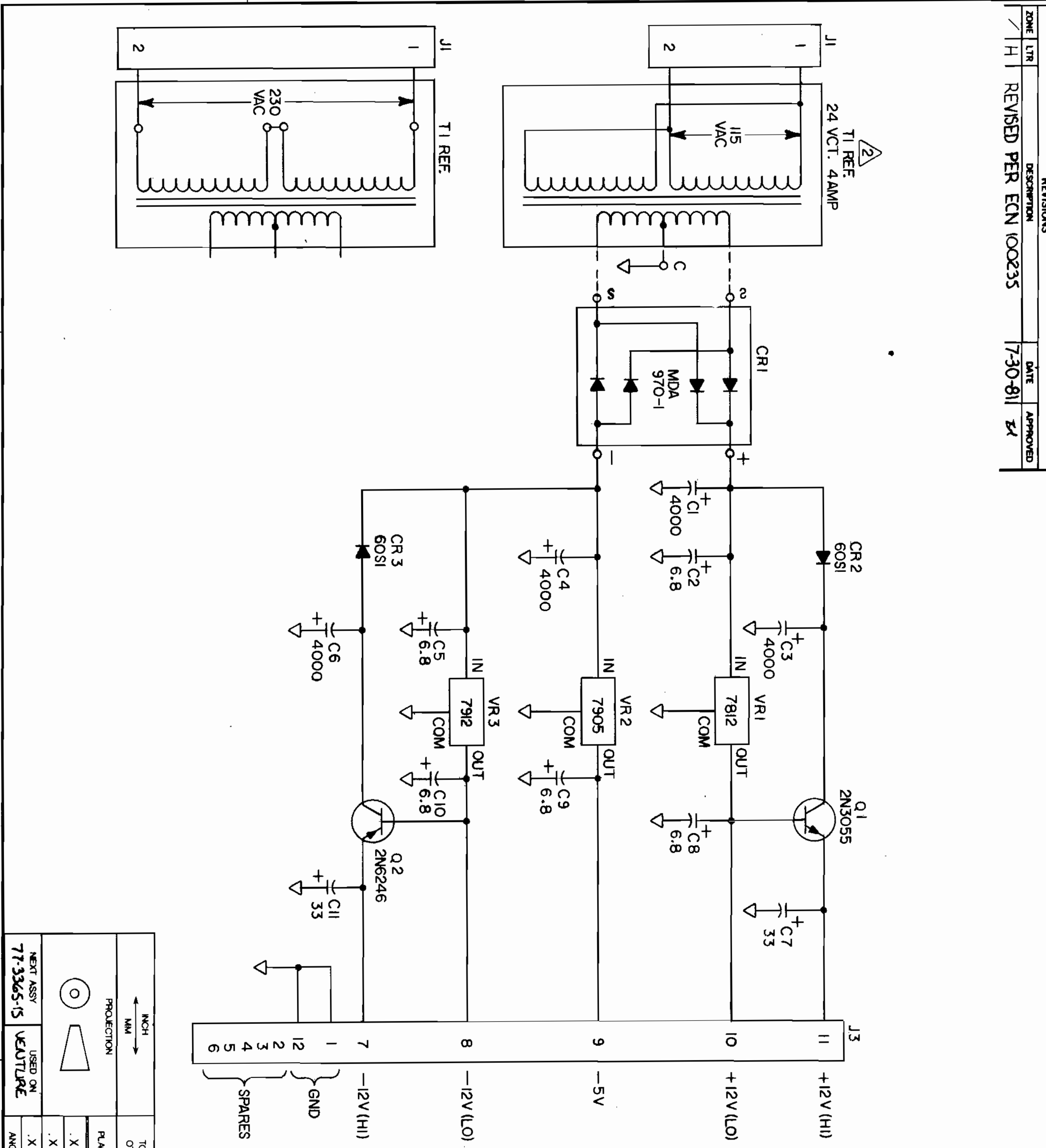
SIZE: D

TITLES-DESCRIPTION: AUDIO/COLOR PCB SCHEMATIC DIAGRAM

SHEET 2 OF 5

DRAWING NO: 77-0007-01

12

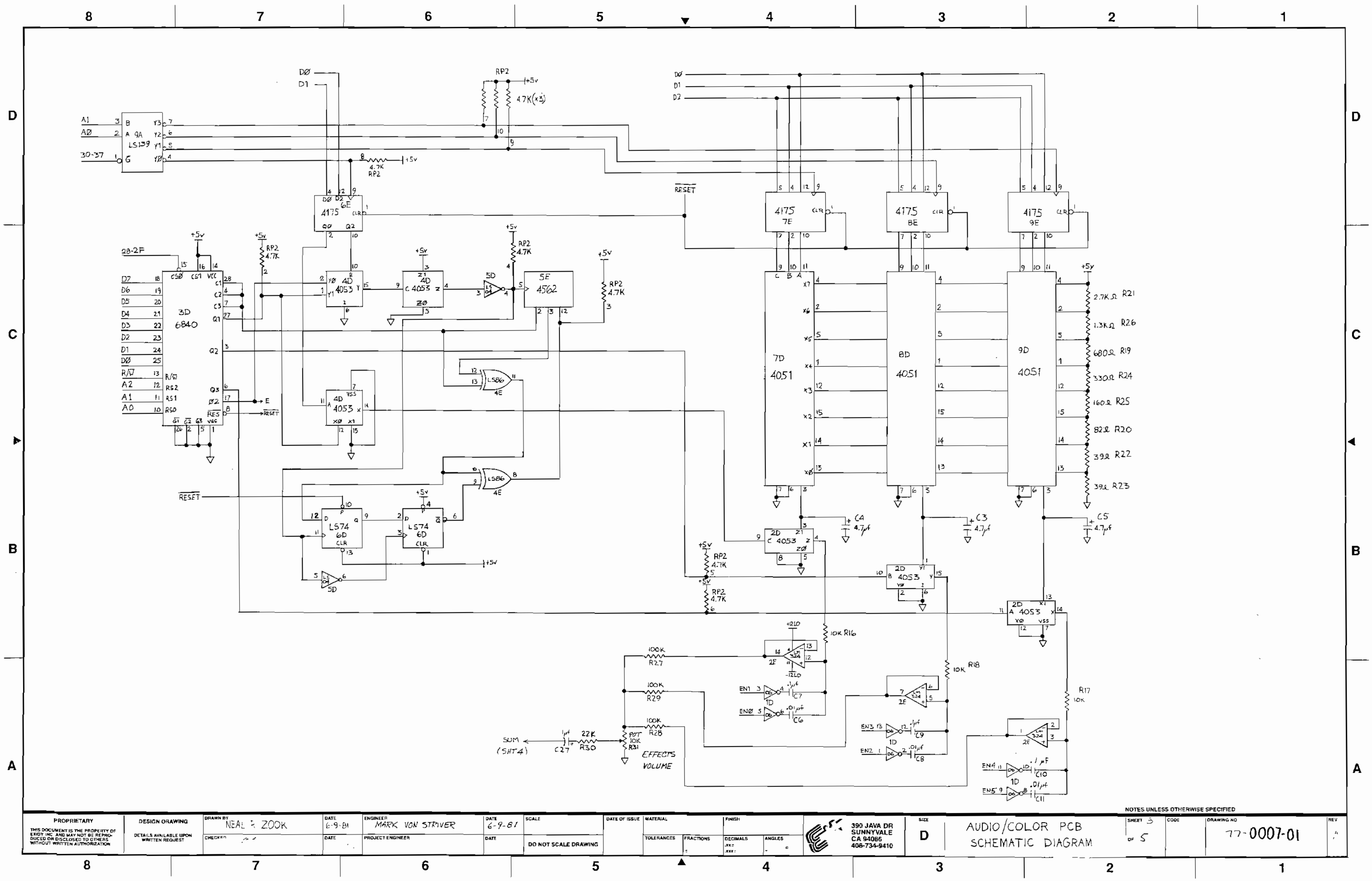



2 SHOWN FOR REFERENCE ONLY

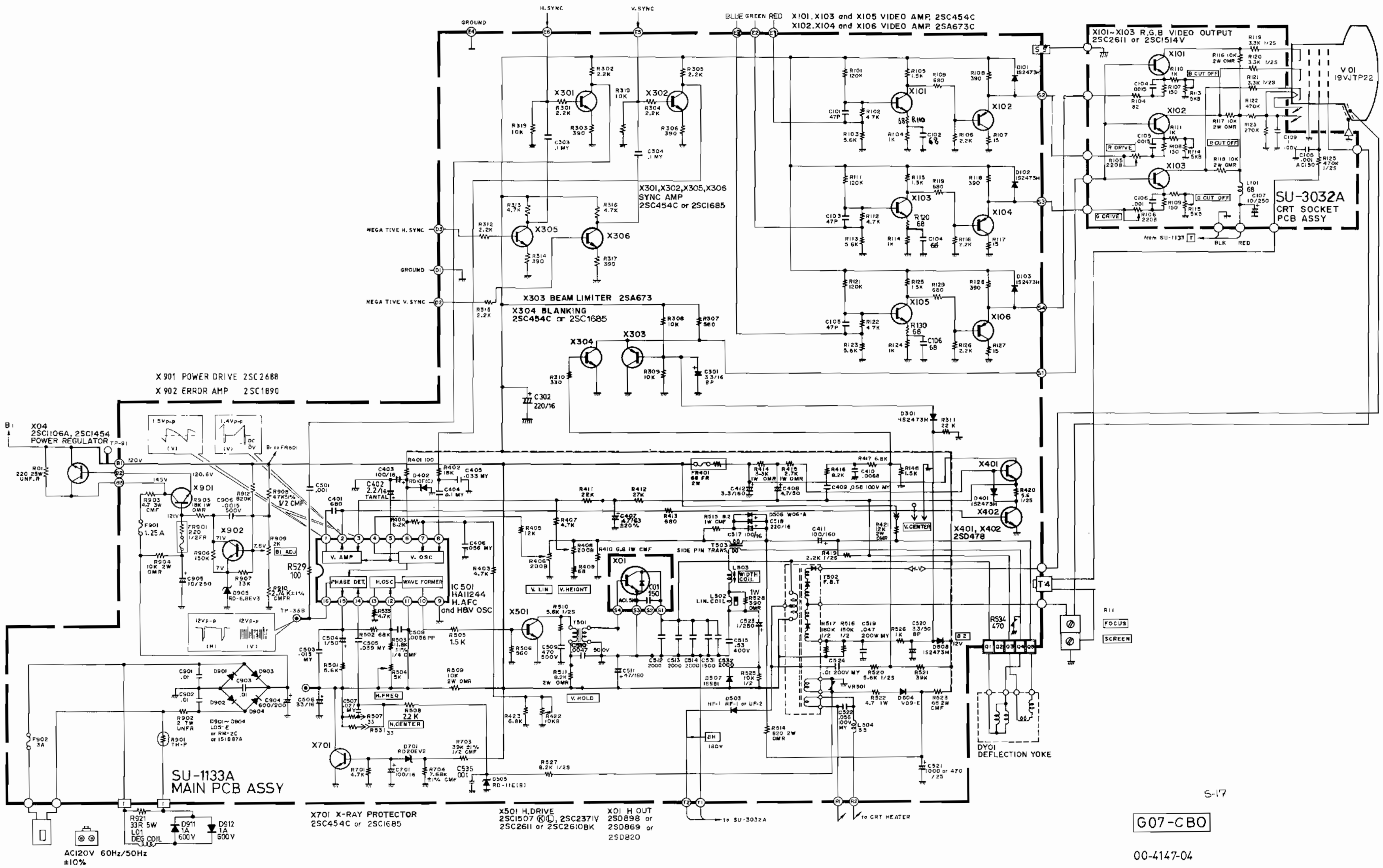
1. ALL CAPACITOR VALUES ARE IN MICROFARADS

NOTES UNLESS OTHERWISE SPECIFIED:

| | | | |
|---|---|---|---|
| Exidy 390 JAVA DR SUNNYVALE CA 94086 408-734-9410 | MATERIAL | FINISH | |
| TOLERANCES | FRACTIONS ± | ANGLES ± | DECIMALS .XX± .XXX± |
| DRAWN BY | | DATES 7-10-81 | |
| CHECKED | | 7/15/81 | |
| ENGINEER | | 7/15/81 | |
| PROJECT ENGINEER | | | |
| PROPRIETARY THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION. | DESIGN DRAWING DETAILS AVAILABLE UPON WRITTEN REQUEST | | |
| SIZE C | CODE VT | SCALE — | |
| TITLE/DESCRIPTION ELECTRICAL SCHEMATIC, UNIVERSAL POWER SUPPLY | SHEET 1 OF 1 | | |
| DRAWING NO. 77-3365-11 | REV H | | |
| DO NOT SCALE DRAWING | | | |



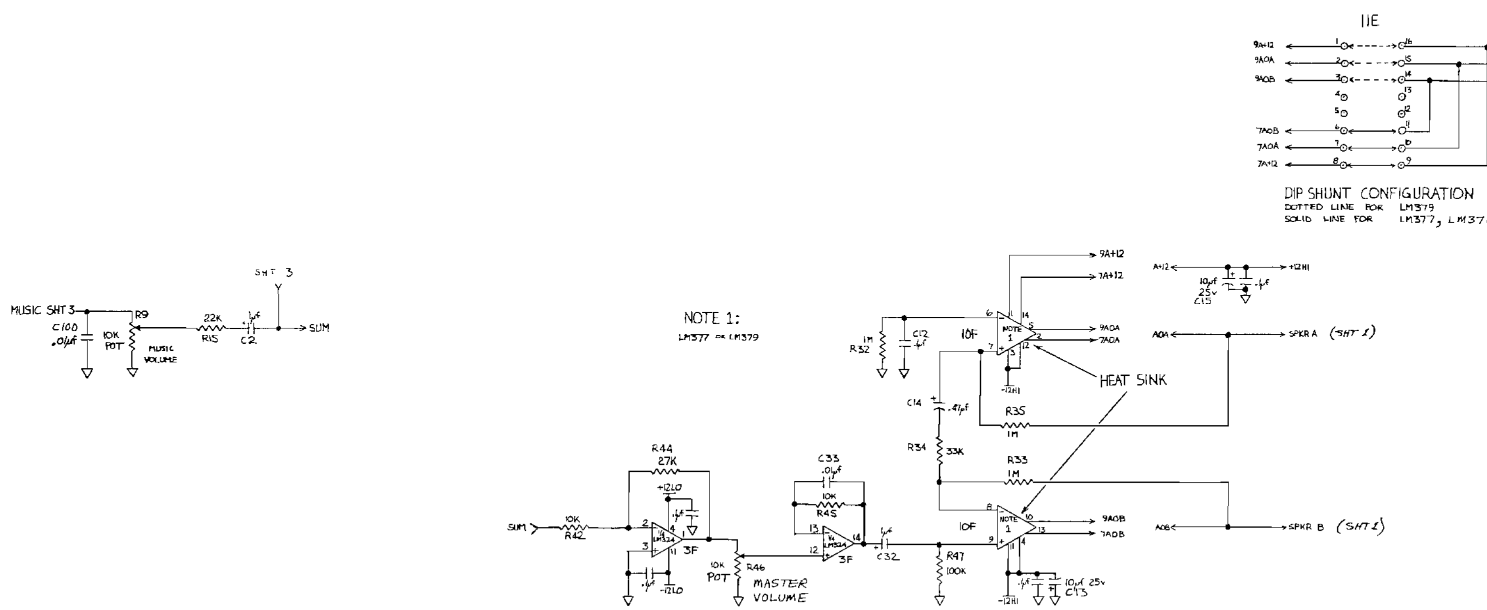
AUDIO/COLOR PCB
SCHEMATIC DIAGRAM
77-0007-01
SHEET 3 OF 5
SIZE D
390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410
DRAWN BY NEAL F. ZOOK 6-9-81
ENGINEER MARK VON STRIVER 6-9-81
DO NOT SCALE DRAWING
NOTES UNLESS OTHERWISE SPECIFIED
PROPRIETARY
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DESIGN DRAWING
DETAILS AVAILABLE UPON WRITTEN REQUEST
3D 6840
LS139 9A
4175 6E
4175 7E
4175 8E
4175 9E
7D 4051
8D 4051
9D 4051
5E 4562
LS74 6D
LS86 4E
2D 4053
4D 4053
EFFECTS VOLUME
SUM (SHT 4)
RESET




S-17

G07-CBO

00-4147-04

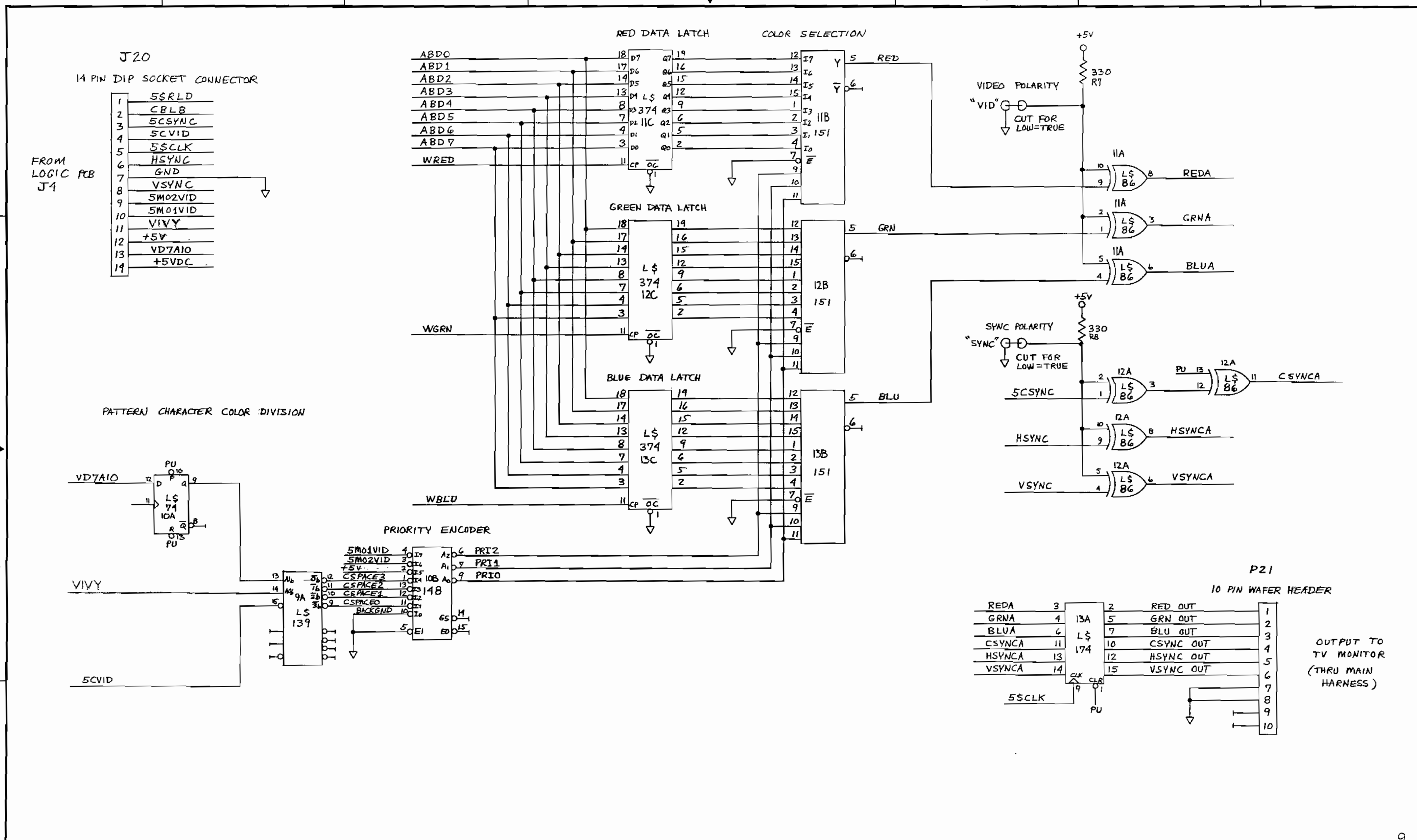



NOTES UNLESS OTHERWISE SPECIFIED

| | | | | |
|---|---|---|---|---|
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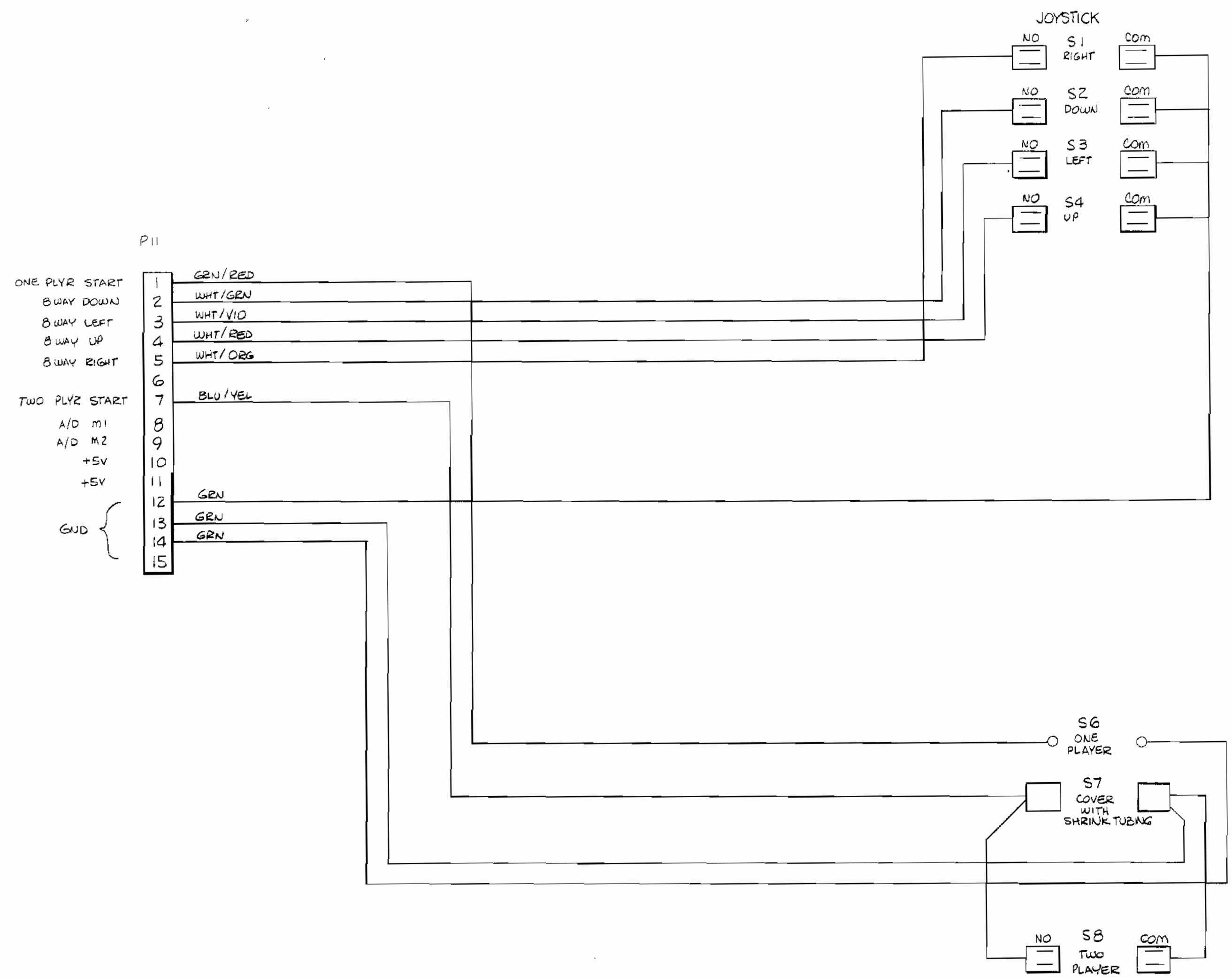
390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

SIZE D — AUDIO/COLOR PCB SCHEMATIC DIAGRAM — SHEET 4 OF 5 — DRAWING NO. 77-0007-01



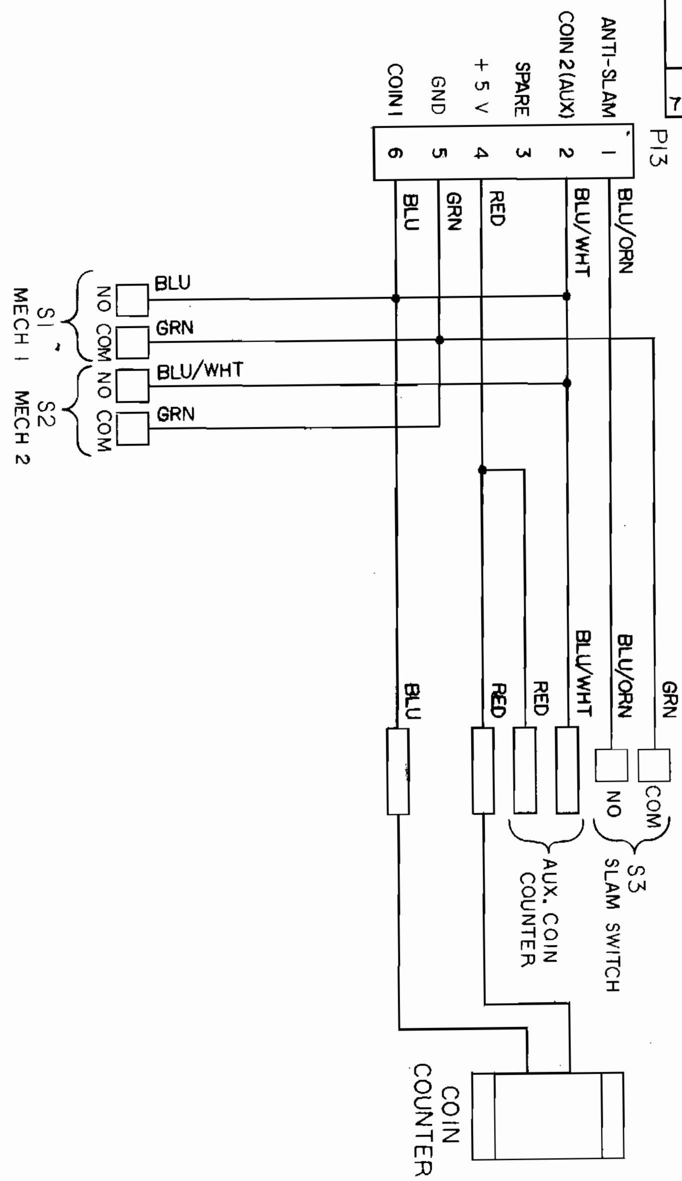

9

| PROPRIETARY | DRAWN BY | DATE | ENGINEER | DATE | SHEET | OF | NEXT ASSEMBLY | USED ON | | SIZE | TITLE/DESCRIPTION | SHEET | CODE | DRAWING NO. | REV |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| THIS DOCUMENT IS THE PROPERTY OF EXIDY INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION. | AKY | 6-7-81 | AKY | 6-7-81 | 5 | 5 | | | 390 JAVA DR SUNNYVALE CA 94086 408-734-9410 | D | AUDIO/COLOR PCB SCHEMATIC DIAGRAM | 5 of 5 | | 77-0007-01 | A |
| | CHECKED | DATE 5-10-82 | PROJECT ENGINEER AKY | DATE 6-7-81 | | | | | | | | | | | |




NOTES UNLESS OTHERWISE SPECIFIED:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| PROPRIETARY<br>THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION. | DESIGN DRAWING<br>DETAILS AVAILABLE UPON WRITTEN REQUEST | DRAWN BY McKENNA<br>CHECKED P.C. | DATE 5-6-82<br>DATE 5-11-82 | ENGINEER<br>PROJECT ENGINEER | DATE 5 6 82<br>DATE 5-11-82 | SCALE ~<br>DO NOT SCALE DRAWING | DATE OF ISSUE | MATERIAL MAKE FROM 71-2391-10<br>TOLERANCES FRACTIONS DECIMALS ANGLES | FINISH |
| 390 JAVA DR<br>SUNNYVALE<br>CA 94086<br>408-734-9410 | SIZE D | TITLES/DESCRIPTION<br>MODIFICATION DWG -<br>WIRING DIAGRAM - C. P. HARNESS | SHEET 1 OF 1 | CODE | DRAWING NO. 49-0001-00 | REV. | | | |




| INCH ↔ MM | TOLERANCES UNLESS OTHERWISE SPECIFIED | | |
|---|---|---|---|
| PROJECTION | PLACES | INCH | MM |
| | .X | + | + |
| | .XX | + | + |
| NEXT ASSY 71-2444-10 / USED ON VENTURE | .XXX | + | + |
| | ANGLES | + | + |

BISHOP GRAPHICS, INC. REORDER NO. 1464

REVISIONS

| ZONE | LTR | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|---|
| / | A | REVISED PER ECN 100235 | 7-30-81 | BA |
| — | B | REVISED PER ECN 100255 | 8/10/81 | BA |

NOTES UNLESS OTHERWISE SPECIFIED:


Exidy
390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

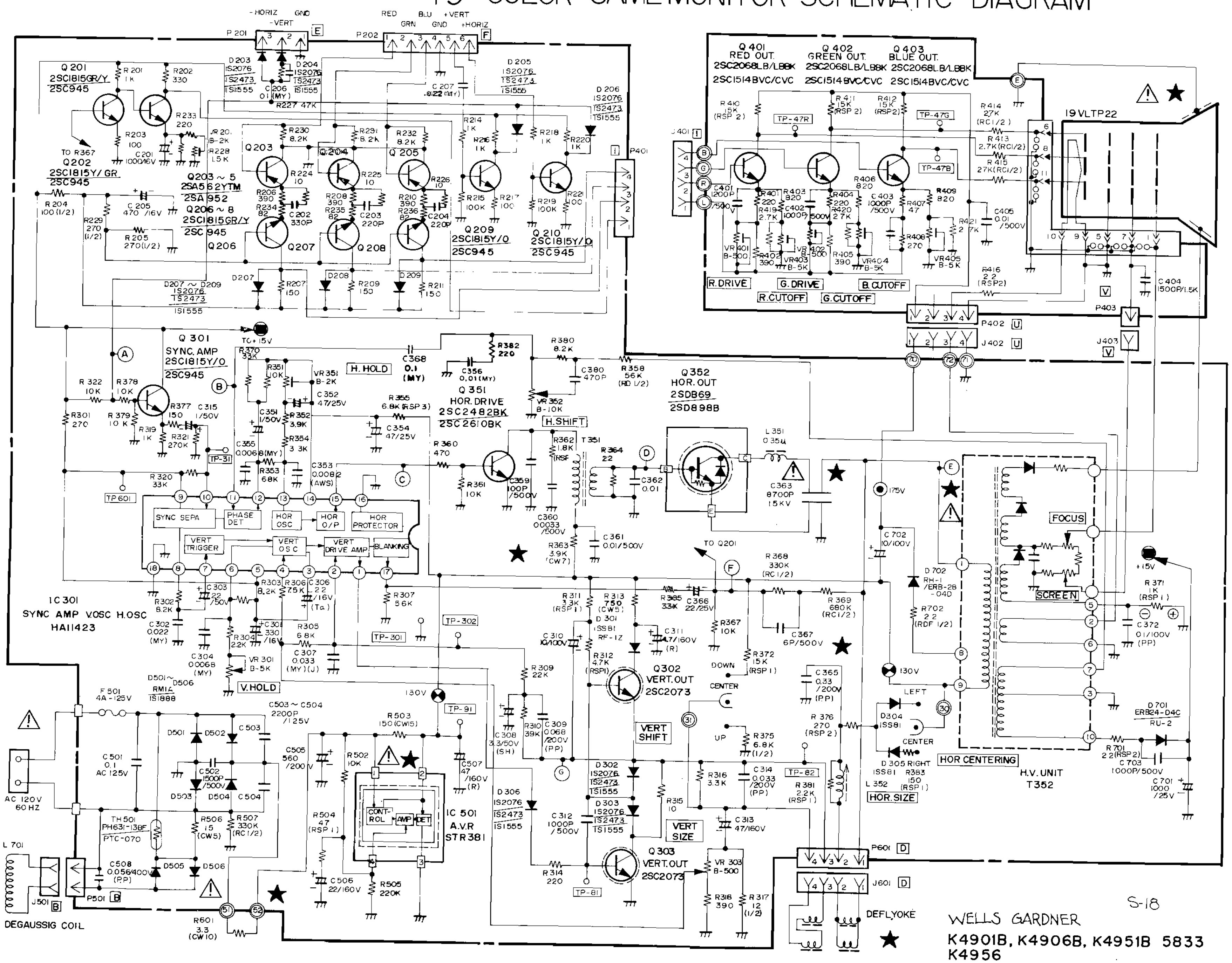

| MATERIAL | FINISH | DRAWN BY | | DATES | SIZE | TITLE/DESCRIPTION | SHEET |
|---|---|---|---|---|---|---|---|
| | | DRAWN BY | | 7-21-81 | C | WIRING DIAGRAM - UNIV. COIN DOOR HARNESS | 1 OF 1 |
| | | CHECKED | | 7/24/81 | CODE | DRAWING NO. | REV |
| | | ENGINEER | | | VT | 71-2449-10 | B |
| TOLERANCES | | PROJECT ENGINEER | | 7/27/81 | SCALE | | |
| FRACTIONS ± | ANGLES ± | | | | | | |
| DECIMALS .XX± | .XXX± | | | | | | |



DESIGN DRAWING
DETAILS AVAILABLE UPON WRITTEN REQUEST

DO NOT SCALE DRAWING

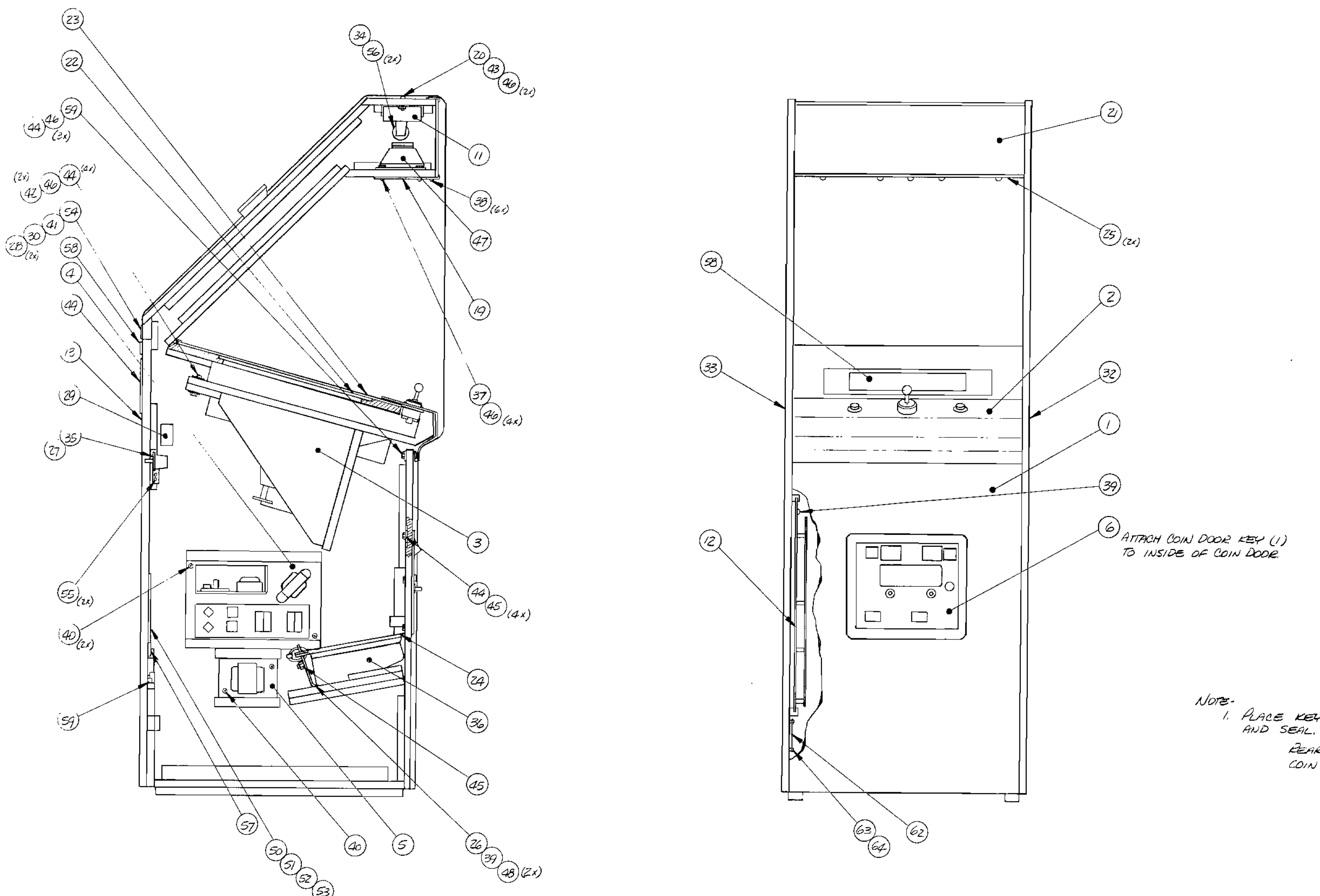
# 19" COLOR GAME MONITOR SCHEMATIC DIAGRAM



S-18

WELLS GARDNER

K4901B, K4906B, K4951B 5833
K4956



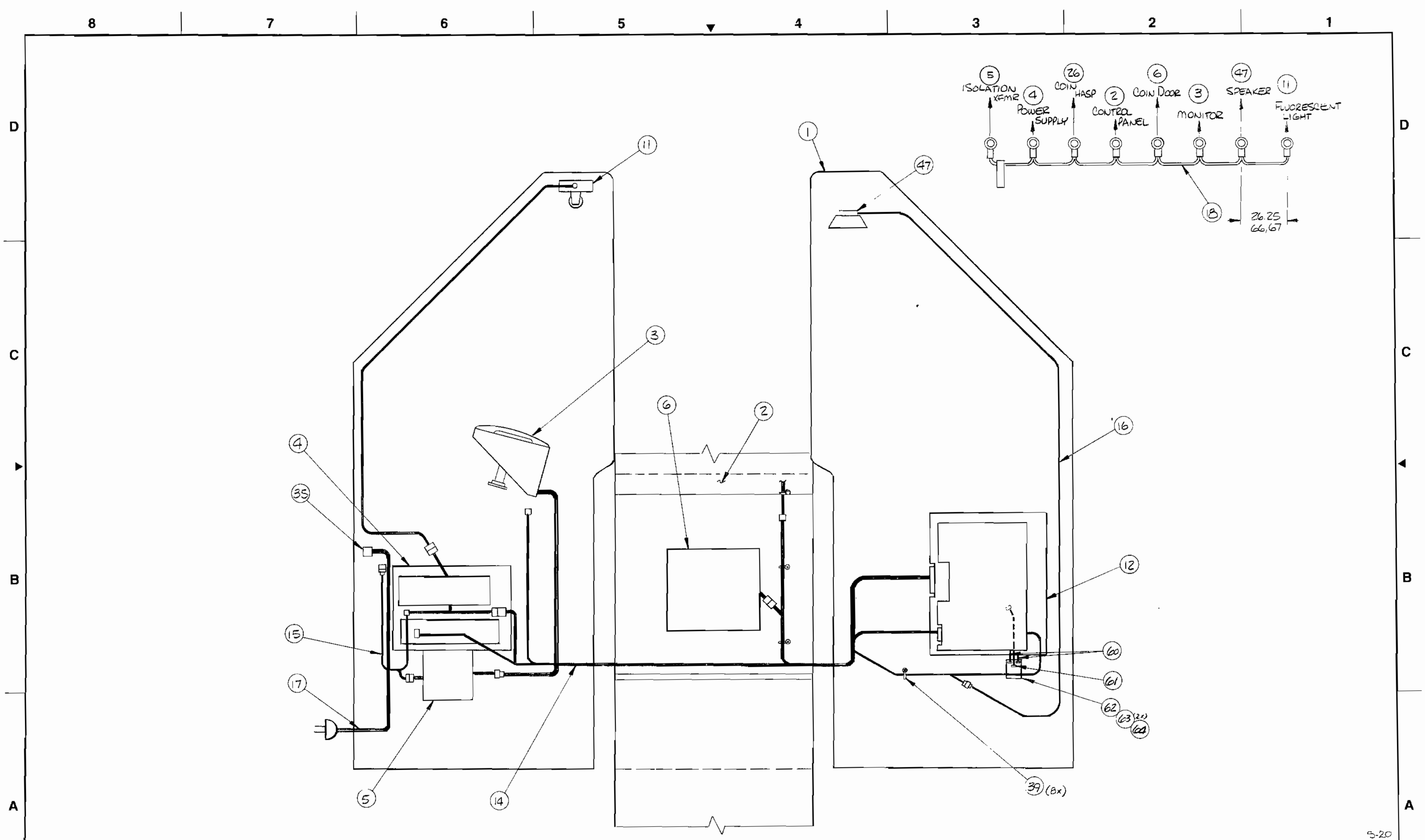

NOTE-
1. PLACE KEYS IN BAG (ITEM 49) AND SEAL.
REAR DOOR - (2)
COIN DOOR - (1)

FOR PARTS LIST SEE P/L 98-0001-00

S-19

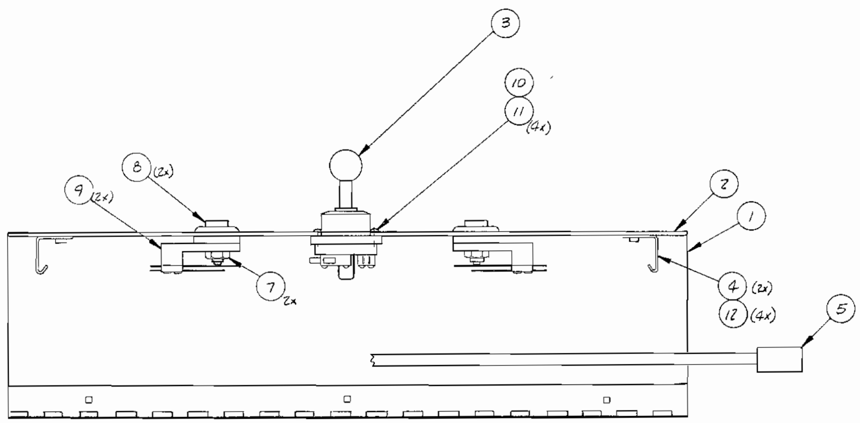
NOTES UNLESS OTHERWISE SPECIFIED:

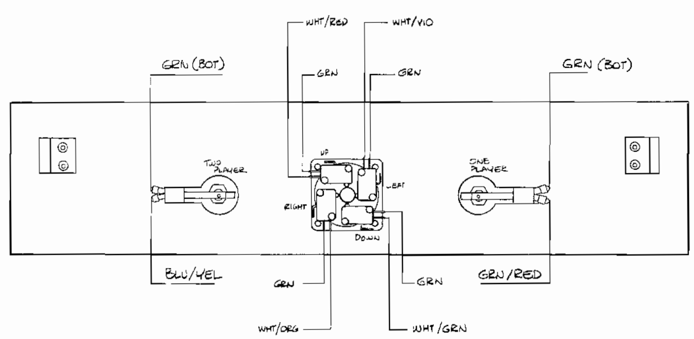
| PROPRIETARY | DESIGN DRAWING | DRAWN BY | DATE | ENGINEER | DATE | SCALE | DATE OF ISSUE | MATERIAL | FINISH | | SIZE | TITLES/DESCRIPTION | SHEET | CODE | DRAWING NO. | REV. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
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| | | CHECKED | DATE | PROJECT ENGINEER [signature] | 5-11-82 | DO NOT SCALE DRAWING | | TOLERANCES | FRACTIONS ± / DECIMALS .XX ± .XXX ± / ANGLES ± 0 | | | | | | | |




NOTES UNLESS OTHERWISE SPECIFIED:

| PROPRIETARY | DESIGN DRAWING | DRAWN BY | DATE | ENGINEER | DATE | SCALE | DATE OF ISSUE | MATERIAL | FINISH | | SIZE | TITLES/DESCRIPTION | SHEET | CODE | DRAWING NO. | REV |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION | DETAILS AVAILABLE UPON WRITTEN REQUEST | McKenna | 5-6-82 | | | | | | | 390 JAVA DR SUNNYVALE CA 94086 408-734-9410 | D | FINAL ASSEMBLY-PEPPER | 2 OF 2 | | 98-0001-00 | |
| | | CHECKED | DATE | PROJECT ENGINEER [signature] | DATE 5-21-82 | DO NOT SCALE DRAWING | | TOLERANCES | FRACTIONS ± / DECIMALS .XX± .XXX± / ANGLES ± ° | | | | | | | |




3. THE FINISHED PANEL SHALL BE FREE FROM DEFECTS WHICH DEGRADE THE OVERALL APPEARANCE. SCRATCHES, ABRASIONS, OR OTHER SURFACE IMPERFECTIONS ARE POSSIBLE CAUSE FOR REJECTION OF PART.

2. THE BOND BETWEEN FILM AND METAL PANEL SHALL BE PERMANENT. ALL SURFACES, CORNERS & EXPOSED EDGES SHALL BE SECURELY ADHERED. THE FINISHED PANEL SHALL BE FREE FROM DEFECTS WHICH COULD CONTRIBUTE TO PREMATURE DELAMINATION. TRAPPED CONTAMINANTS, CRACKS, BUBBLES, WRINKLES, OR BRIDGING IN CORNER RADII ARE PROBABLE CAUSE FOR REJECTION OF PARTS.

1. REGISTRATION OF FILM TO METAL PANEL SHALL BE WITHIN .03 OF THE CENTERLINE POSITIONING OF HOLE DETAILS. FILM OVERLAP AT EXPOSED EDGES OF PANEL SHALL NOT EXCEED .03. ALL HOLES OR PROFILE CUTOUTS, SHALL BE CLEAR & FREE OF FILM OBSTRUCTION.

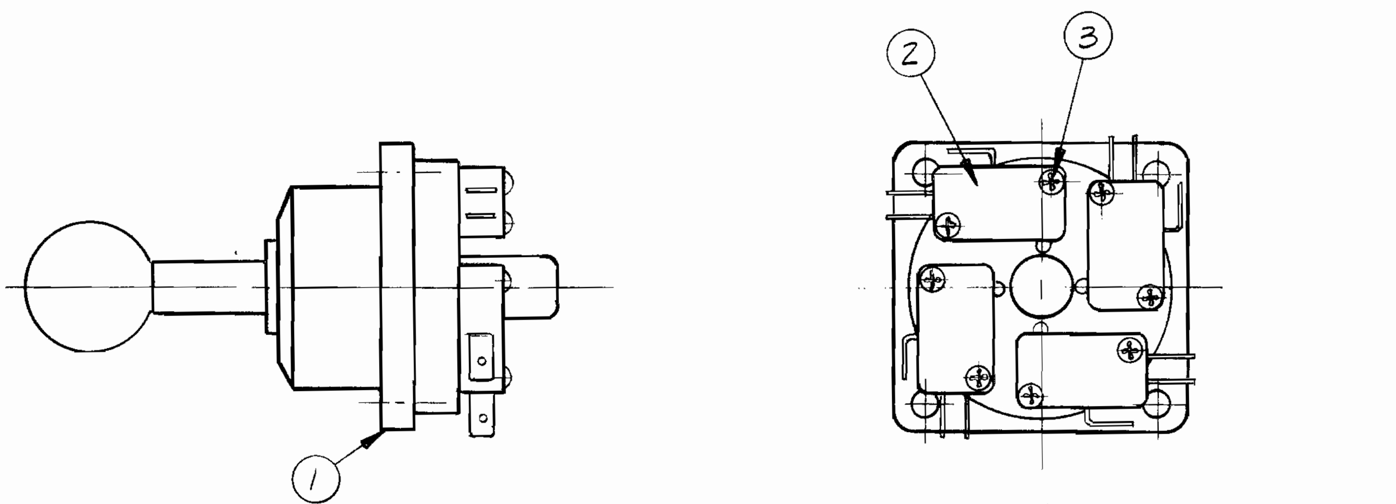
S-21

NOTES UNLESS OTHERWISE SPECIFIED:

| PROPRIETARY | DESIGN DRAWING | DRAWN BY | DATE | ENGINEER | DATE | SCALE | DATE OF ISSUE | MATERIAL | FINISH | | SIZE | TITLE/DESCRIPTION | SHEET | CODE | DRAWING NO. | REV. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION. | DETAILS AVAILABLE UPON WRITTEN REQUEST | McKENNA | 5-6-82 | [illegible] | 5-6-82 | HALF | | | | 390 JAVA DR SUNNYVALE CA 94086 408-734-9410 | D | CONTROL PANEL ASSY (PEPPER) | 1 OF 1 | | 90-0002-0J | |
| | | CHECKED | DATE | PROJECT ENGINEER | DATE | DO NOT SCALE DRAWING | | TOLERANCES FRACTIONS ± | DECIMALS .XX ± .XXX ± | ANGLES ± ° | | | | | | |
| | | | | [illegible] | [illegible] | | | | | | | | | | | |

| VERSION | MICROSWITCH USED |
|---|---|
| -01 | EXIDY 48-5013-00 MICROSWITCH-MODIFIED |
| -02 | MILTAC 10(3)A 250V (EUROPEAN) |
| -03 | |

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | REV. | DESCRIPTION | DATE | APPROVED |
| | | | | |




| ITEM | PART NUMBER | DESCRIPTION | QTY |
|---|---|---|---|
| 3 | 52-6057-00 | SCREW · SELF TAPPING · PH PAN HD | 8 |
| 2 | SEE CHART | MICROSWITCH | 4 |
| 1 | 95-0001-00 | JOY STICK | 1 |

NOTES UNLESS OTHERWISE SPECIFIED

DEC. / M.M.

THIRD ANGLE PROJECTION

MATERIAL
FINISH
FILLETS MAX
BREAK CORNERS
MACHINE FINISH

TOLERANCES UNLESS NOTED
DIMENSION INCH mm
.X = ±
.XX = ±
.XXX = ±
ANGLES ±

| | | DATE |
|---|---|---|
| DFTG | [signature] | 5-5-82 |
| CHK | | |
| ENGR | [signature] | 5-5-82 |
| PROJ ENGR | [signature] | 5-11-82 |

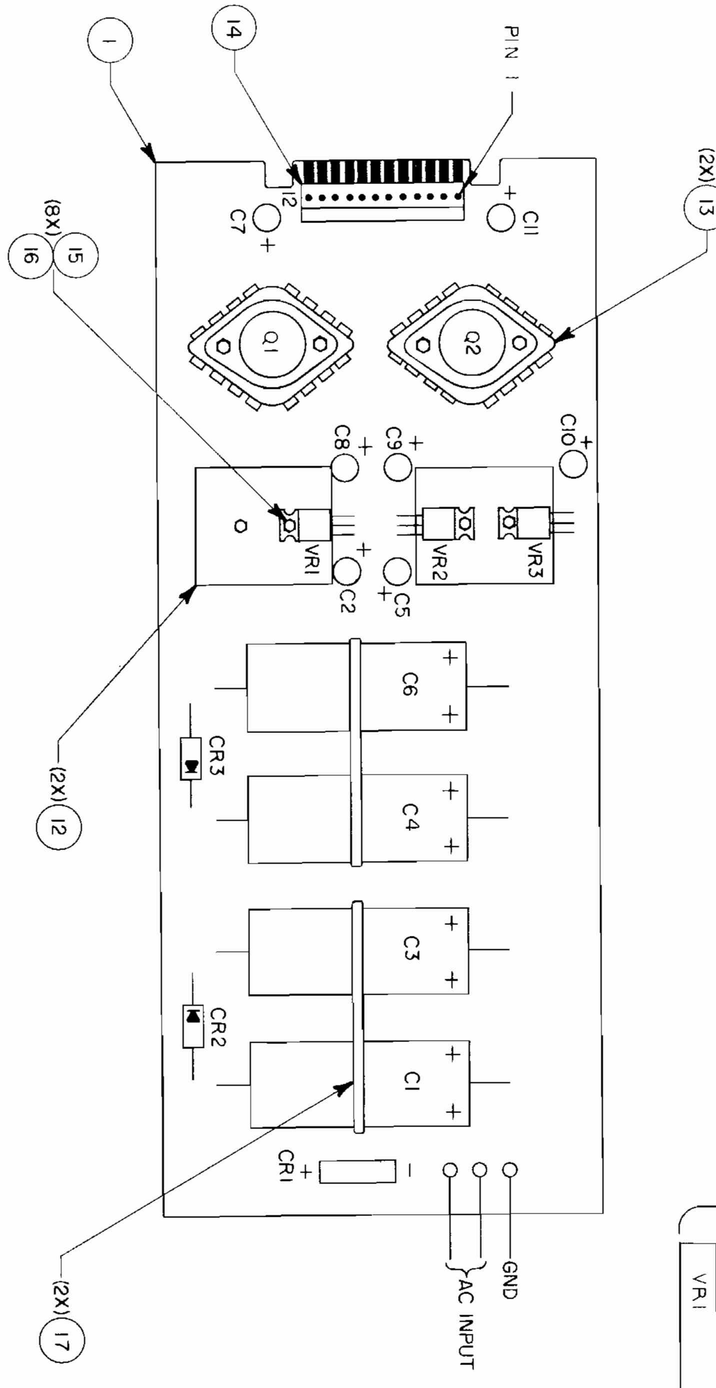
PROPRIETARY
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390 JAVA DR
SUNNYVALE, CA 94086
408-734-9410

TITLE: ASSEMBLY - JOY STICK

B | CODE IDENT NO. | 90-0001-XX

SCALE FULL | NEXT | SHT




| INCH / MM PROJECTION | |
|---|---|
| NEXT ASSY | USED ON |
| 38-51 34-40 | [illegible] |

TOLERANCES UNLESS OTHERWISE SPECIFIED

| PLACES | INCH | MM |
|---|---|---|
| .X | ± | ± |
| .XX | ± | ± |
| .XXX | ± | ± |
| ANGLES | ± | ± |

REVISIONS

| ZONE | LTR | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|---|
| | I | REVISED PER ECN 100235 | 8-4-81 | [illegible] |

COMPONENT LIST ⚠1

| REF. DESIG. | ITEM NO. |
|---|---|
| C1,3,4,6 | 2 |
| C2,5,8,9,10 | 4 |
| C7,11 | 3 |
| CR1 | 6 |
| CR2,3 | 5 |
| Q1 | 7 |
| Q2 | 8 |
| VR2 | 9 |
| VR3 | 10 |
| VR1 | 11 |

FOR PARTS LIST SEE 77-3365-15

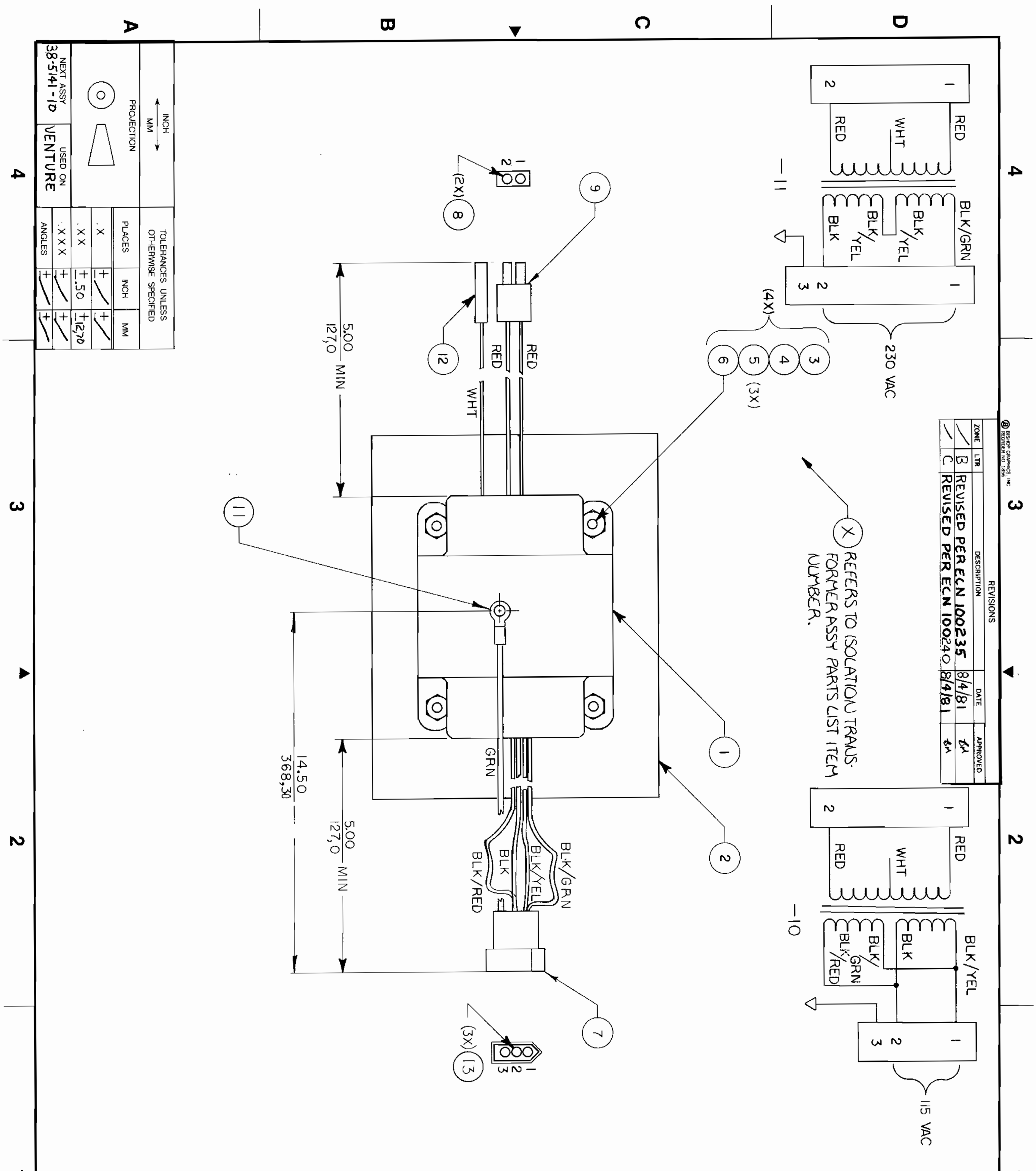
NOTES UNLESS OTHERWISE SPECIFIED:

⚠1 APPLY HEAT TRANSFER COMPOUND TO ITEMS 7 THRU 11

| Exidy 390 JAVA DR SUNNYVALE CA 94086 408-734-9410 | MATERIAL | FINISH | DRAWN BY | DATES 7-9-81 | SIZE C | TITLE/DESCRIPTION UNIVERSAL POWER SUP. PCB ASSY | SHEET OF |
|---|---|---|---|---|---|---|---|
| | TOLERANCES | | CHECKED | 7/15/81 | CODE VT | DRAWING NO. 77-3365-15 | REV I |
| | FRACTIONS ± | ANGLES ± | ENGINEER | 7/15/81 | | | |
| | DECIMALS .XX ± | .XXX ± | PROJECT ENGINEER | | SCALE 1/1 | DO NOT SCALE DRAWING | |



DESIGN DRAWING DETAILS AVAILABLE UPON WRITTEN REQUEST




FOR PARTS LIST 38-5136-XX

NOTES UNLESS OTHERWISE SPECIFIED:

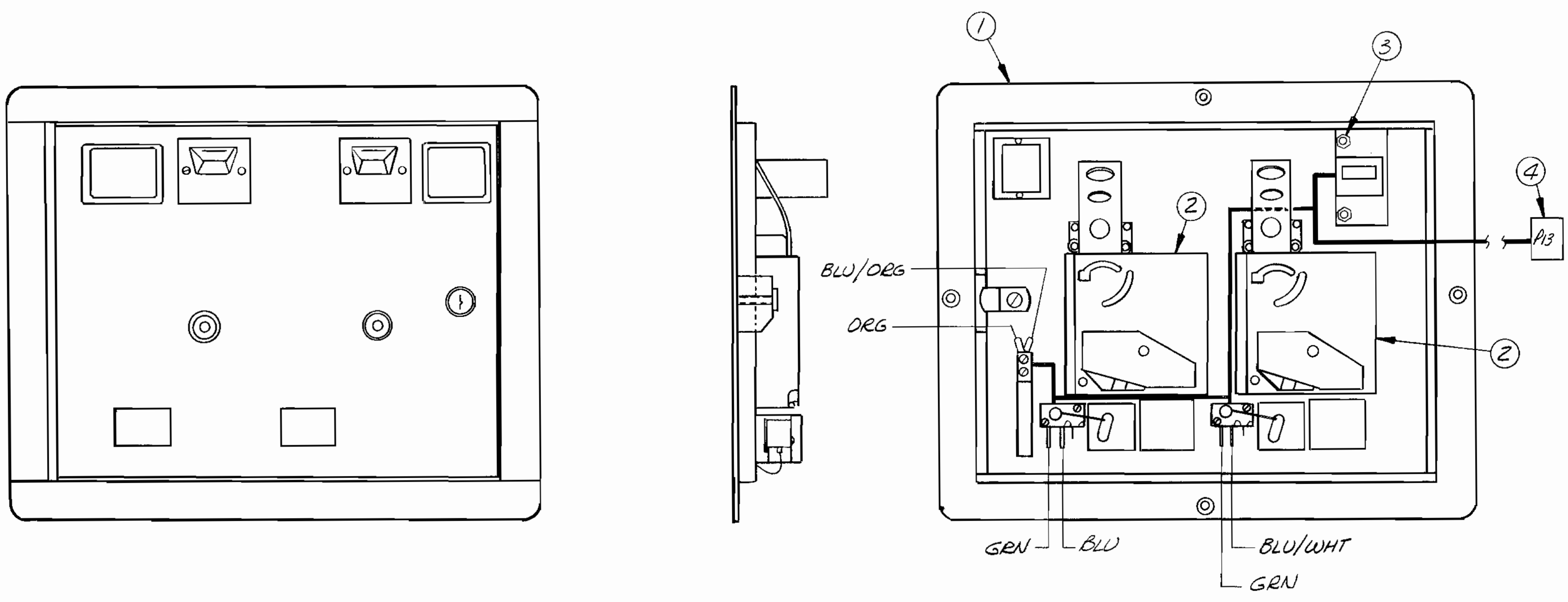
390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

| | | | |
|---|---|---|---|
| MATERIAL | FINISH | DRAWN BY | DATES 6-30-81 |
| | | CHECKED | 7/3/81 |
| TOLERANCES | | ENGINEER | |
| FRACTIONS ± | ANGLES ± | PROJECT ENGINEER | |
| DECIMALS .XX ± | .XXX ± | | |

PROPRIETARY
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DESIGN DRAWING
DETAILS AVAILABLE UPON WRITTEN REQUEST

| | | | |
|---|---|---|---|
| SIZE C | TITLE/DESCRIPTION TRANSFORMER ASSY, ISOLATION | | SHEET 1 OF 1 |
| CODE VT | DRAWING NO. 38-5136-XX | | REV C |
| SCALE 1/1 | DO NOT SCALE DRAWING | | |




| ITEM | PART NUMBER | DESCRIPTION | QTY |
|---|---|---|---|
| 4 | 71-2444-10 | UNIV COIN HARNESS ASSY | 1 |
| 3 | 74-3502 | NUT, KEP #6-32 | 2 |
| 2 | 90-0031-00 | COIN ACCEPTOR-MOD | 2 |
| 1 | 90-0032-00 | COIN DOOR-MOD | 1 |

REVISIONS

| ZONE | REV. | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|---|
| | | | | |

NOTES UNLESS OTHERWISE SPECIFIED

390 JAVA DR
SUNNYVALE, CA 94086
408-734-9410

TITLE: COIN DOOR ASSEMBLY

DFTG: McKenna  DATE: 6-9-82
CHK
ENGR
PROJ ENGR

CODE IDENT NO. C  90-0035-00

SCALE ~  NEXT  SHT

MATERIAL / FINISH / FILLETS MAX / BREAK CORNERS / MACHINE FINISH

DEC. / M.M.

THIRD ANGLE PROJECTION

TOLERANCES UNLESS NOTED
DIMENSION
.X = ±
.XX = ±
.XXX = ±
ANGLES ±

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